Das Elektronik I Team

- Prof. Dr. Eberhard Riedle
  Fakultät für Physik, LS für BioMolekulare Optik

  Eberhard.Riedle@physik.uni-muenchen.de

- Prof. Dr. Roland Kersting: Festkörperphysik
- Dr. Alexander Mlynek: Platinenherstellung

- „Multisim 14“ Simulationsprogramm

- homepage:

  http://www.bmo.physik.uni-muenchen.de/~riedle/Elektronik_I/

Stabilization and precise calibration of a continuous-wave difference frequency spectrometer by use of a simple transfer cavity

E. Riedle,[a),b)] S. H. Ashworth,[b)] J. T. Farrell, Jr., and D. J. Nesbitt[c)]
Joint Institute for Laboratory Astrophysics, University of Colorado and National Institute of Standards and Technology, Boulder, Colorado 80309-0440

(Received 15 July 1993; accepted for publication 24 September 1993)

A novel, simple, and inexpensive calibration scheme for a continuous-wave difference frequency spectrometer is presented, based on the stabilization of an open transfer cavity by locking onto the output of a polarization stabilized HeNe laser. High frequency, acoustic fluctuations of the transfer cavity length are compensated with a piezoelectric transducer mounted mirror, while long term drift in cavity length is controlled by thermal feedback. A single mode Ar^+ laser, used with a single mode ring dye laser in the difference frequency generation of 2–4 μm light, is then locked onto a suitable fringe of this stable cavity, achieving a very small long term drift and furthermore reducing the free running Ar^+ linewidth to about 1 MHz. The dye laser scan provides tunability in the difference frequency mixing process, and is calibrated by marker fringes with the same stable cavity. Due to the *absolute* stability of the marker cavity, precise frequency determination of near infrared molecular transitions is achieved via interpolation between these marker fringes. It is shown theoretically that the residual error of this scheme due to the dispersion of air in the transfer cavity is quite small, and experimentally that a frequency precision on the order of 1 MHz per hour is routinely obtained with respect to molecular transitions.

bisher 75 x zitiert

Stabilization of the Difference Frequency Spectrometer

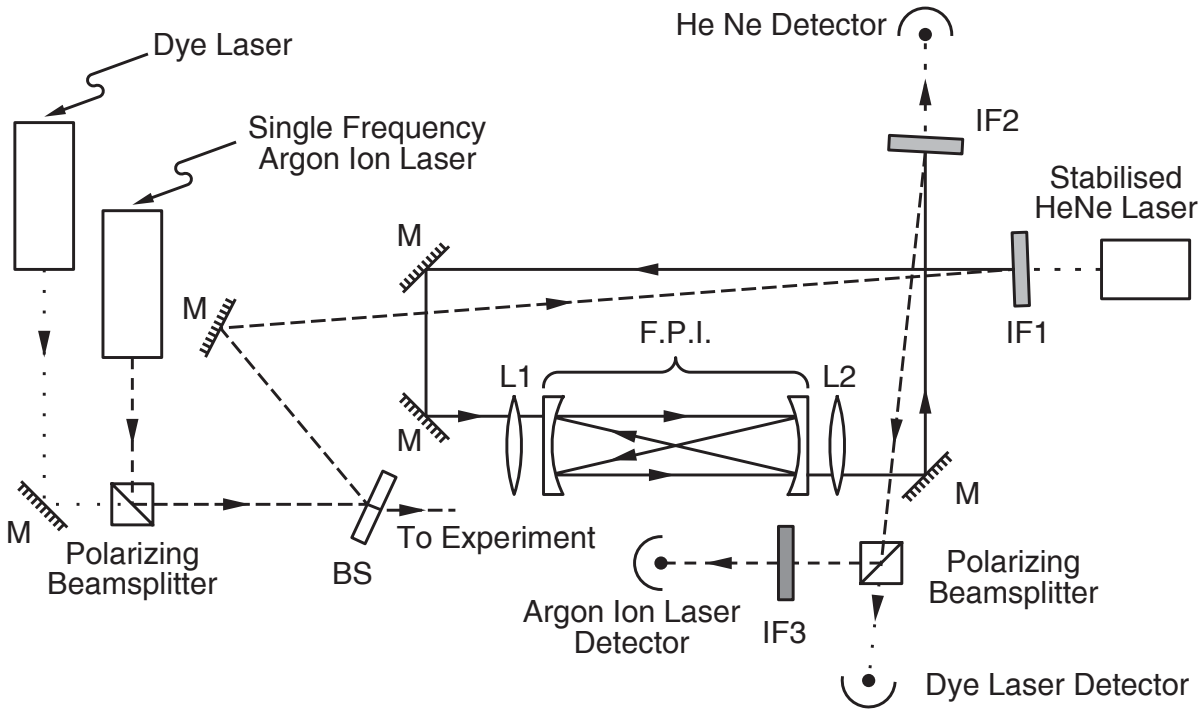
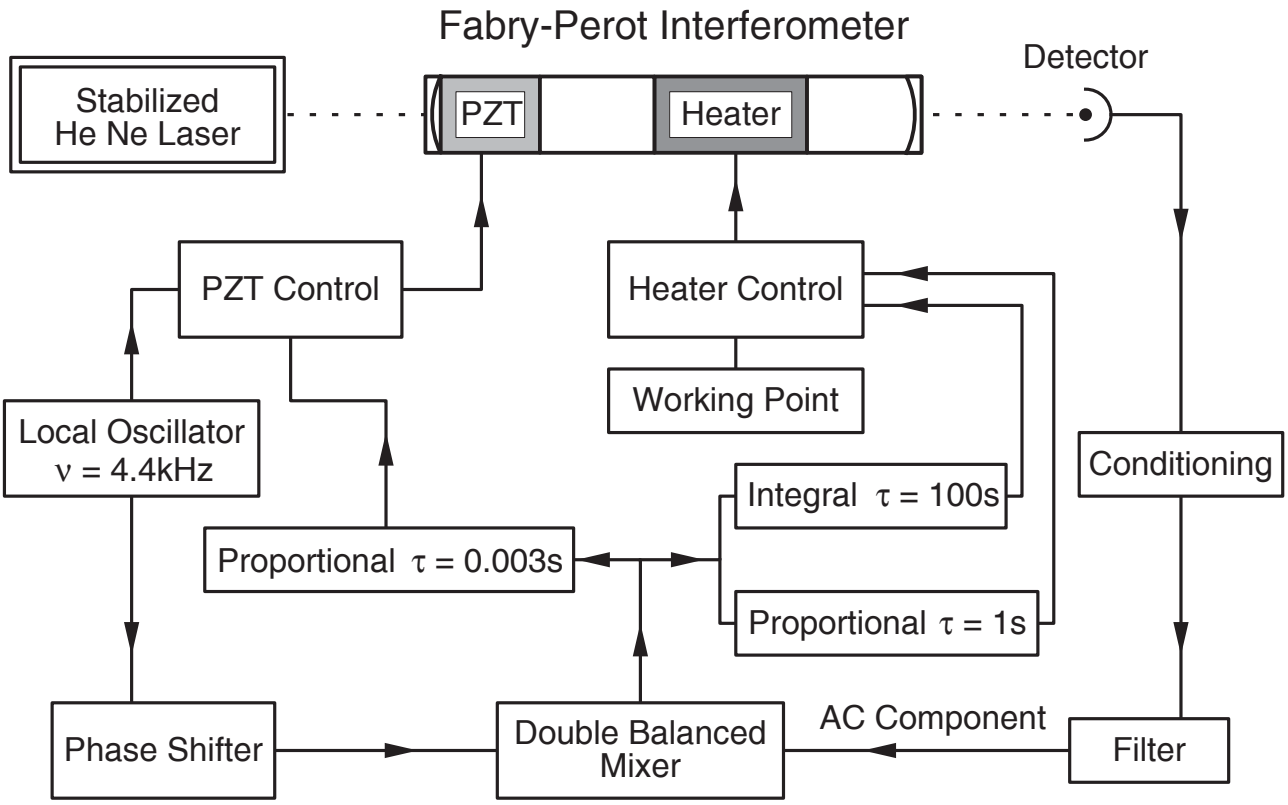
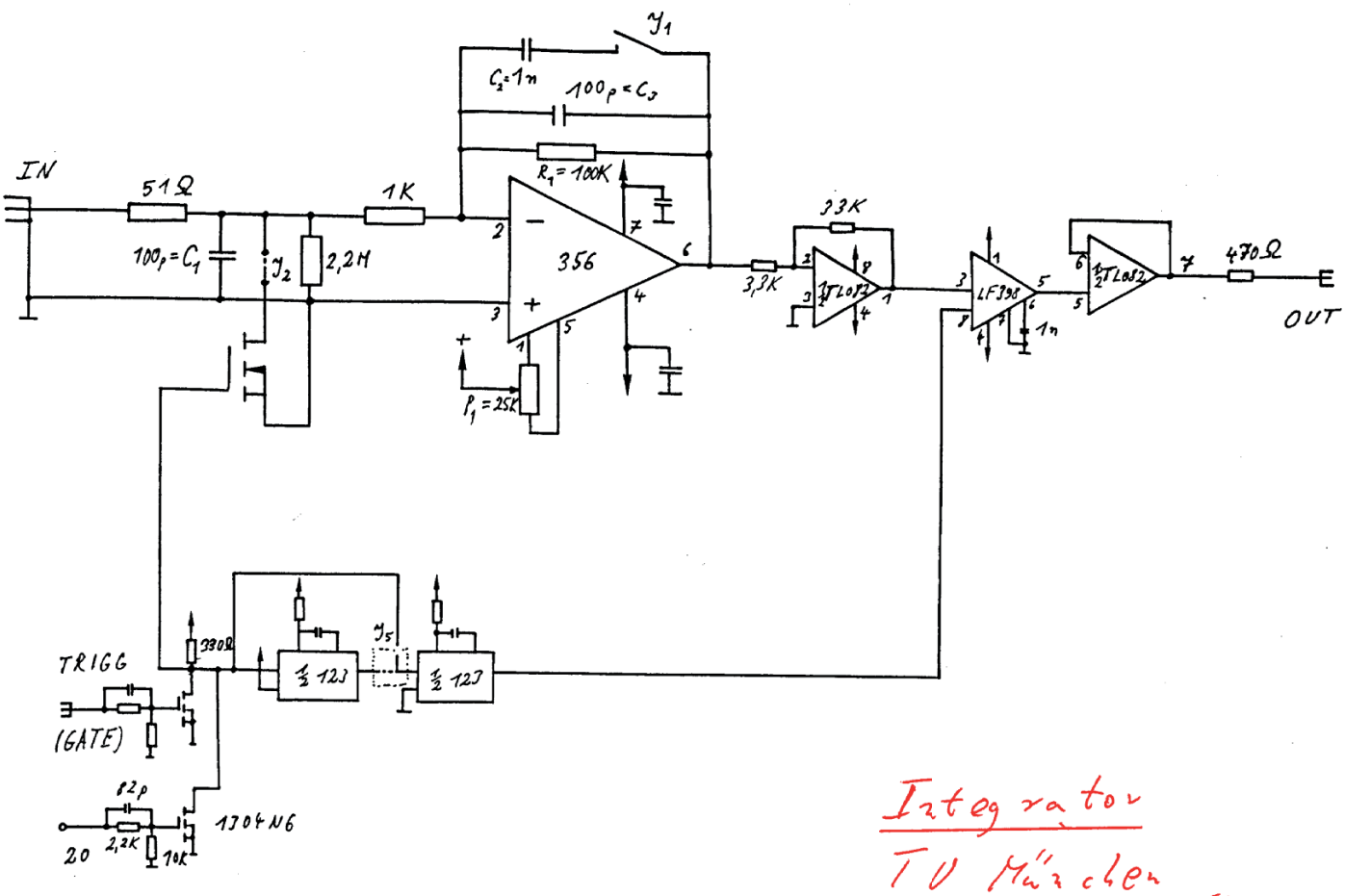


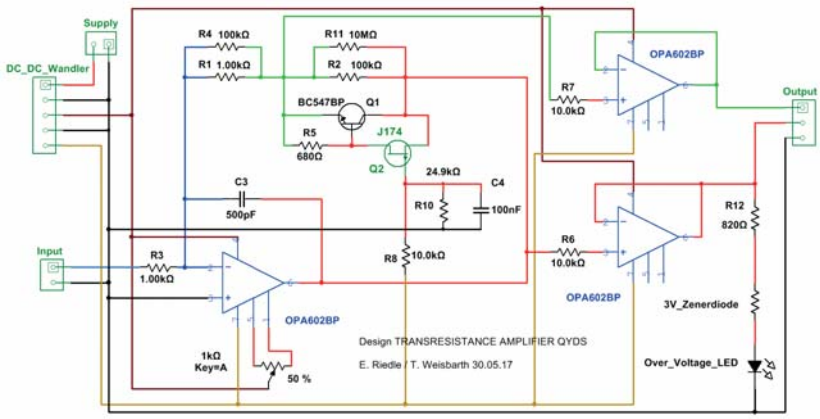
figure 1 E. Riedle et al., 'Stabilization and ...'

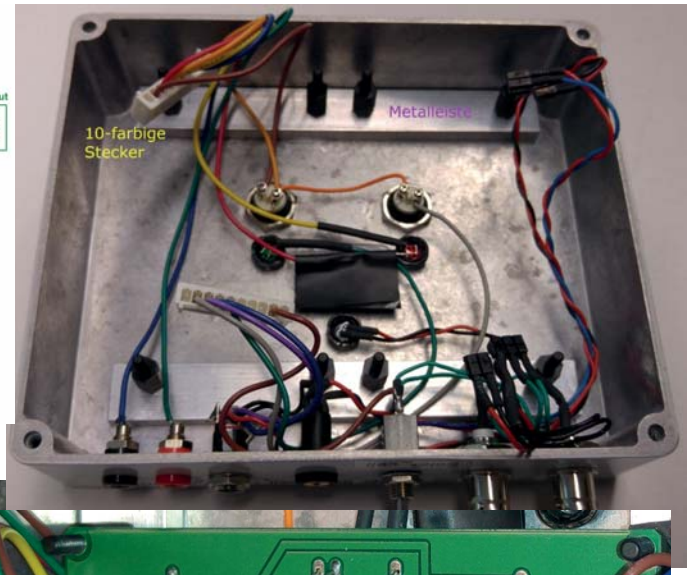
Locking of The Transfer Cavity

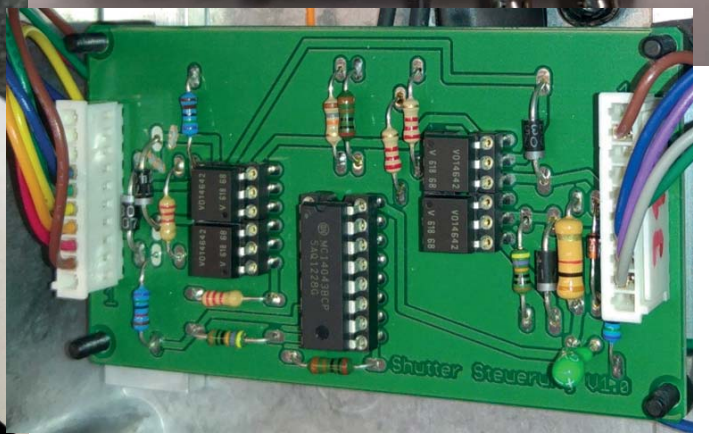




QYDS electronics : shutter control and I/U converter for solar cell







Elektronik I, WS 2017/18 (E. Riedle)

0. Vorstellung und Einleitung

I. Lineare passive Bauelemente

1) Grundbegriffe, Widerstände, Kondensatoren, Spulen
2) Lineare Netzwerke - Reduzierung, Wheatstone'sche Brücke
3) Komplexe Amplituden in linearen Netzwerken
4) Anwendungen und Beispiele - Filterschaltungen, Schwingkreise

II. Netzwerke mit aktiven Bauelementen

1) Aktive Bauelemente - Spannungs- und Stromquelle, Ersatzschaltbilder
2) Zweipolquelle
3) Kreisstromverfahren, Knotenspannungen, Numerische Verfahren
4) Vierpole - Transformator, Vierpol- oder Filterkette
5) Leitungen, HF-Leitungen, Leitungstransformator etc.
   - Reflexion, Transmission
   - Anwendungen: kurze Pulse, Impedanztransformatoren
   - Oberflächenwellen, HF-Filter

III. Messtechnik und Schaltungssimulation

IV. Halbleiterbauelemente

1) Einleitung mit Kurzübersicht
   - Halbleiter, Dotierung, p-n Übergang
   - Shockley-Gleichung, Durchbruchsmechanismen
2) Dioden - Kenlinienaufnahme etc.
   - NF Dioden: Gleichrichterdiode, Kapazitätsdiode, Z-Diode, Spannungsregler
   - HF Dioden: Oszillatoren, Tunneldiode, Backwarddiode, pin-Diode
3) Transistoren
   - pnp / npn Transistor, Kennlinien, Arbeitspunkt
   - Grundschaltungen: Emitterschaltung, Kollektorschaltung, Basisschaltung
   - Verstärkung: Ruhestromeinstellung, Kleinsignalverstärkung
     Strom-/Spannungs-Gegenkopplung, Bootstrapping
     zweistufiger Verstärker, Differenzverstärker, Darlington-Stufe
   - Transistor als Schalter - ohmsche Last, kapazitive Last, induktive Last
   - FET's: JFET, MOSFET, HEMT, Thyristor, Triac
   - Dimmer, Analogschalter
   - Spannungsregler, Netzteile, Konstantstromquelle

V. Integrierte Schaltungen / Operationsverstärker (OPAMP)

1) Aufbau (3 Stufen) und Funktionsweise
2) Herstellung integrierter Schaltungen
3) Betriebsarten des OPAMP, Mit- und Gegenkopplung, Übertragungskennlinie,
   reale OPAMPs, Auswahl für praktische Anwendungen
4) Übertragungs-charakteristik:
   - Spannungsverstärker (invertierend / nichtinvertierend)
   - Rechenschaltungen: Addierer, Subtrahierer, Differenzierer
     Integrierer, Logarithmierer, Delog., Wurzel, etc.
   - Komparator, Schmitt-Trigger, Sample&Hold
   - U/I Converter, I/U Converter
   - "gated" Integrator (Beispiel; Anwendung)
   - aktive Filter, Instrumentenverstärker
   - Hochspannungsverstärker (Beispiel)
   - Funktionsgeneratoren
   - hochstabile Netzteile
   - Schaltungen mit dem Zeitgeber "555"

VI. Steuerung und Regelung

1) Grundlagen, Zweipunktregler, Dreipunktregler, Bode - Diagramm (Stabilität)
2) Elemente des Regelkreises: Regelstrecke, Meßglied, Stellglied, Regler
3) PID - Regler, Einstellung
4) Beispiel: Fabry-Perot-Stabilisierung
5) PLL (phase-locked-loops)

VII. Optoelektronische Bauelemente

1) Photowiderstände
2) Photodioden, -transistoren; Differenzdetektion
3) Photomultiplier
4) Leuchtdiode, Diodenlaser
5) Optokoppler
6) Anzeigen
7) Akustooptische und elektrooptische Modulatoren

Literatur

1. U. Tietze, Ch. Schenk: " Halbleiterschaltungstechnik "

2. P. Horowitz, W. Hill: " The Art of Electronics "
   Horowitz/Hill: "Die Hohe Schule der Elektronik 1 + 3 " (nur gebraucht verfügbar)

3. E. Hering, K. Bressler, J.Gutekunst: " Elektronik für Ingenieure "

4. H. Hartl, E. Krasser, G. Winkler, W. Pribyl, P. Söser: "Elektronische Schaltungstechnik"

Multisim 14: National Instruments
http://www.ni.com/multisim/
Studentenlizenzen € 23,74

?

Mathcad Prime 2.0 - [AKADEMISCH] - C:\VorlesungenRd\Elektronik\Elektronik_I_13_14\KW042\Mi_Einfuehrung\beam_propagation_1.mcdx

Rechnen | Eingabe/Ausgabe | Funktionen | Matrizen/Tabellen | Diagramme | Formatierung | Berechnung | Dokument | Erste Schritte

Rechnen | Lösungsblock | Textblock | Textfeld | Bild | Bereich löschen | Operatoren | Symbole | Programmierung | Konstanten | Symbolische Mathematik | Beschriftungen (kein/e) | Tiefgestellt | Einheiten | Einheitensystem: SI | Basiseinheiten | Zwischenablage

Bereiche | Operatoren und Symbole | Stil | Einheiten

beam_propagation_1

$$M_d(d) := \begin{bmatrix} 1 & d \\ 0 & 1 \end{bmatrix} \qquad M_f(f) := \begin{bmatrix} 1 & 0 \\ -\frac{1}{f} & 1 \end{bmatrix}$$

Berechnung der Fokusposition einer Linsenkombination

Gleichungsblock

Nebenbedingungen

Schätzwerte

$$d_{2f} := 150 \qquad r_1 := \begin{bmatrix} 0.1 \\ 0 \end{bmatrix}$$

$$r_1 = M_d(d_{2f}) \cdot M_f(-150) \cdot M_d(d_{12}) \cdot M_f(200) \cdot r_0$$

$$\widehat{r_1^{1}} = 0$$

$$\begin{bmatrix} d_{2f} \\ r_1 \end{bmatrix} := \mathbf{find}(d_{2f}, r_1)$$

$$d_{2f} = 240.6 \qquad r_1 = \begin{bmatrix} 7.551 \cdot 10^{-20} \\ -0.004 \end{bmatrix}$$

Berechnung von w0 aus λ und der "Divergenz", also der Neigung r´

$$d_{tot} := d_{12} + d_{2f} = 365.6 \qquad w_0 := \frac{\lambda}{\pi \cdot \left(-\widehat{r_1^{2}}\right)} \cdot M2 = [38.9]\ \mu m$$

LF155/LF156/LF157 Series Monolithic JFET Input Operational Amplifiers

National Semiconductor

December 1994

LF155/LF156/LF157 Series Monolithic JFET Input Operational Amplifiers

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast setting time, low voltage and current noise and a low 1/f noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (5,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

Common Features

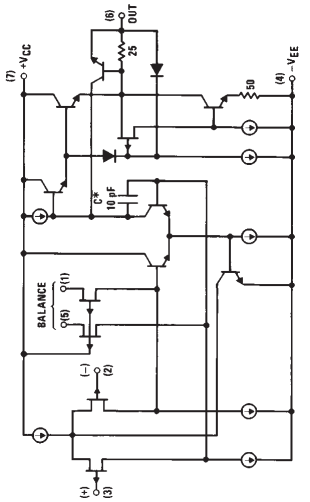
(LF155A, LF156A, LF157A)

Low input bias current	30 pA
Low Input Offset Current	3 pA
High input impedance	$10^{12}\Omega$
Low input offset voltage	1 mV
Low input offset voltage temp. drift	3 μV/°C
Low input noise current	0.01 pA/√Hz
High common-mode rejection ratio	100 dB
Large dc voltage gain	106 dB

Uncommon Features

	LF155A	LF156A	LF157A ($A_V = 5$)	Units
Extremely fast settling time to 0.01%	4	1.5	1.5	μs
Fast slew rate	5	12	50	V/μs
Wide gain bandwidth	2.5	5	20	MHz
Low input noise voltage	20	12	12	nV/√Hz

Simplified Schematic



TL/H/5646–1

*3 pF in LF157 series.

BI-FET™, BI-FET II™ are trademarks of National Semiconductor Corporation.

RRD-B30M115/Printed in U. S. A.

DC Electrical Characteristics (Note 3) $T_A = T_j = 25°C$ (Continued)

Symbol	Parameter	Conditions	LF155A/6A/7A			LF355A/6A/7A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15.1 −12		±11	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics $T_A = T_j = 25°C$, $V_S = \pm 15V$

Symbol	Parameter	Conditions	LF155A/355A			LF156A/356A			LF157A/357A			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	LF155A/6A; $A_V = 1$, LF157A; $A_V = 5$	3	5		10	12		 40	 50		V/μs V/μs
GBW	Gain Bandwidth Product			2.5		4	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5			1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz f = 1000 Hz		 25 20			 15 12			 15 12		 nV/√Hz nV/√Hz
i_n	Equivalent Input Noise Current	f = 100 Hz f = 1000 Hz		0.01 0.01			0.01 0.01			0.01 0.01		pA/√Hz pA/√Hz
C_{IN}	Input Capacitance			3			3			3		pF

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF155/6/7			LF255/6/7 LF355B/6B/7B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ Over Temperature		3	5 7		3	5 6.5		3	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5			5		μV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		μV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		3	20 20		3	20 1		3	50 2	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	100 50		30	100 5		30	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2k$ Over Temperature	50 25	200		50 25	200		25 15	200		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$ $V_S = \pm 15V$, $R_L = 2k$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15.1 −12		±11	±15.1 −12		+10	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 8)

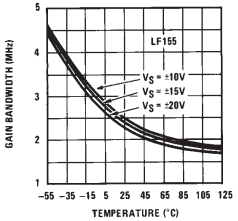
	LF155A/6A/7A	LF155/6/7	LF355B/6B/7B LF255/6/7	LF355/6/7 LF355A/6A/7A
Supply Voltage	±22V	±22V	±22V	±18V
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
T_{jMAX}				
H-Package	150°C	150°C	115°C	115°C
N-Package			100°C	100°C
M-Package			100°C	100°C
Power Dissipation at $T_A = 25°C$ (Notes 1 and 9)				
H-Package (Still Air)	560 mW	560 mW	400 mW	400 mW
H-Package (400 LF/Min Air Flow)	1200 mW	1200 mW	1000 mW	1000 mW
N-Package			670 mW	670 mW
M-Package			380 mW	380 mW
Thermal Resistance (Typical) θ_{JA}				
H-Package (Still Air)	160°C/W	160°C/W	160°C/W	160°C/W
H-Package (400 LF/Min Air Flow)	65°C/W	65°C/W	65°C/W	65°C/W
N-Package			130°C/W	130°C/W
M-Package			195°C/W	195°C/W
(Typical) θ_{JC}				
H-Package	23°C/W	23°C/W	23°C/W	23°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Soldering Information (Lead Temp.)				
Metal Can Package				
Soldering (10 sec.)	300°C	300°C	300°C	300°C
Dual-In-Line Package				
Soldering (10 sec.)		260°C	260°C	260°C
Small Outline Package				
Vapor Phase (60 sec.)			215°C	215°C
Infrared (15 sec.)			220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.				
ESD tolerance				
(100 pF discharged through 1.5 kΩ)	1000V	1000V	1000V	1000V

DC Electrical Characteristics (Note 3) $T_A = T_j = 25°C$

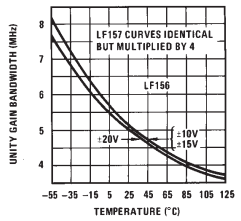
Symbol	Parameter	Conditions	LF155A/6A/7A			LF355A/6A/7A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ Over Temperature		1	2 2.5		1	2 2.3	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3	5		3	5	μV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		μV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		3	10 10		3	10 1	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	50 25		30	50 5	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2k$ Over Temperature	50 25	200		50 25	200		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$ $V_S = \pm 15V$, $R_L = 2k$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V

Typical AC Performance Characteristics

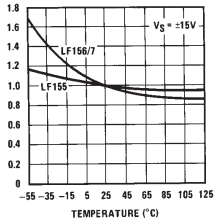
Gain Bandwidth



Gain Bandwidth

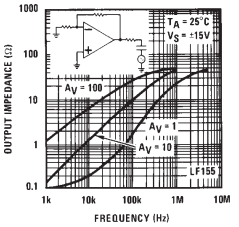


Normalized Slew Rate

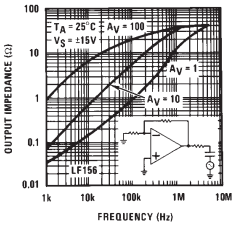


TL/H/5646–4

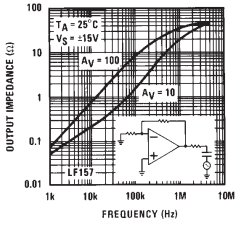
Output Impedance



Output Impedance

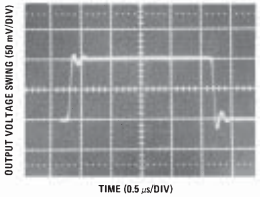


Output Impedance



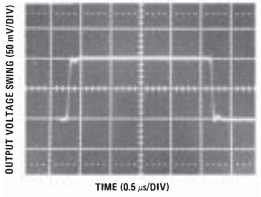
TL/H/5646–12

LF155 Small Signal Pulse Response, A_V = +1



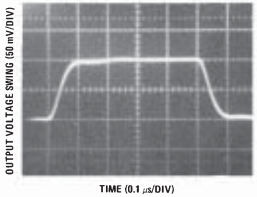
TL/H/5646–5

LF156 Small Signal Pulse Response, A_V = +1



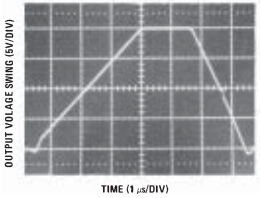
TL/H/5646–6

Small Signal Pulse Response, A_V = +5



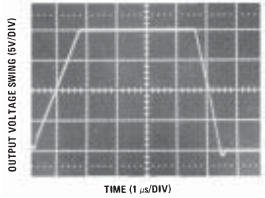
TL/H/5646–7

LF155 Large Signal Pulse Response, A_V = +1



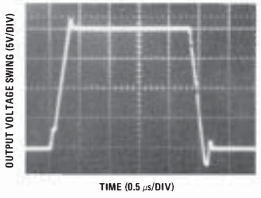
TL/H/5646–8

LF156 Large Signal Pulse Response, A_V = +1



TL/H/5646–9

LF157 Large Signal Pulse Response, A_V = +5



TL/H/5646–10

DC Electrical Characteristics $T_A = T_j = 25°C$, $V_S = \pm 15V$

Parameter	LF155A/155, LF255, LF355A/355B		LF355		LF156A/156, LF256/356B		LF356A/356		LF157A/157 LF257/357B		LF357A/357		Units
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Supply Current	2	4	2	4	5	7	5	10	5	7	5	10	mA

AC Electrical Characteristics $T_A = T_j = 25°C$, $V_S = \pm 15V$

Symbol	Parameter	Conditions	LF155/255/ 355/355B	LF156/256, LF356B	LF156/256/ 356/356B	LF157/257, LF357B	LF157/257/ 357/357B	Units
			Typ	Min	Typ	Min	Typ	
SR	Slew Rate	LF155/6: A_V = 1, LF157: A_V = 5	5	7.5	12	30	50	V/µs V/µs
GBW	Gain Bandwidth Product		2.5		5		20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5		1.5	µs
e_n	Equivalent Input Noise Voltage	R_S = 100Ω f = 100 Hz f = 1000 Hz	 25 20		 15 12		 15 12	 nV/√Hz nV/√Hz
i_n	Equivalent Input Current Noise	f = 100 Hz f = 1000 Hz	0.01 0.01		0.01 0.01		0.01 0.01	pA/√Hz pA/√Hz
C_{IN}	Input Capacitance		3		3		3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{JMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

	LF155A/6A/7A LF155//6/7	LF255//6/7	LF355A/6A/7A	LF355B/6B/7B	LF355//6/7
Supply Voltage, V_S	±15V ≤ V_S ≤ ±20V	±15V ≤ V_S ≤ ±20V	±15V ≤ V_S ≤ ±18V	±15V ≤ V_S ±20V	V_S = ±15V
T_A	−55°C ≤ T_A ≤ +125°C	−25°C ≤ T_A ≤ +85°C	0°C ≤ T_A ≤ +70°C	0°C ≤ T_A ≤ +70°C	0°C ≤ T_A ≤ +70°C
T_{HIGH}	+125°C	+85°C	+70°C	+70°C	+70°C

and V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5µV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \theta_{jA}$ Pd where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit).

Note 8: Refer to RETS155AX for LF155A, RETS155X for LF155, RETS156AX for LF156A, RETS156X for LF156, RETS157A for LF157A and RETS157X for LF157 military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Application Hints

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

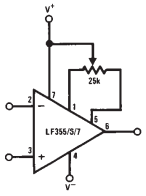
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

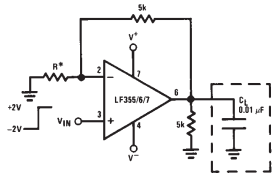
Typical Circuit Connections

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment
- Typical overall drift: 5 μV/°C ±(0.5 μV/°C/mV of adj.)

Driving Capacitive Loads



*LF155/6 R = 5k

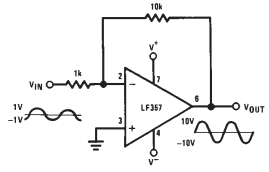
LF157 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \approx 0.01$ μF.

Overshoot ≤ 20%

Settling time (t_s) ≈ 5 μs

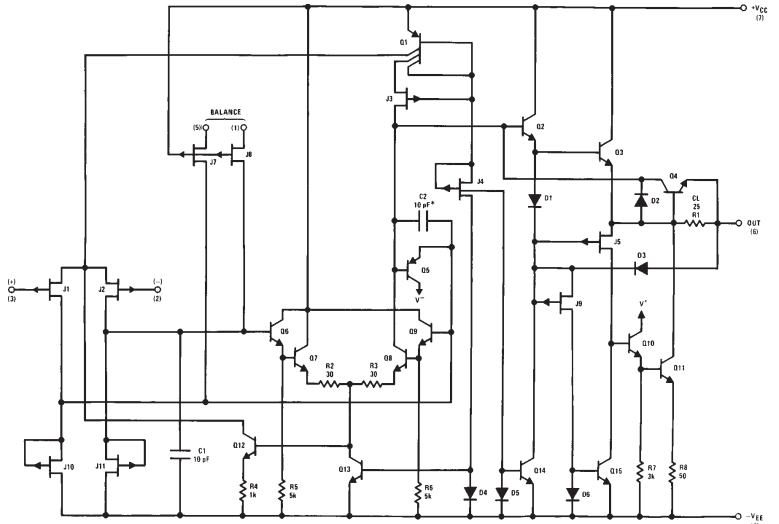
LF157. A Large Power BW Amplifier



TL/H/5646–15

For distortion ≤ 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500 kHz.

Detailed Schematic

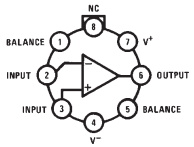


*C = 3 pF in LF157 series.

TL/H/5646–13

Connection Diagrams (Top Views)

Metal Can Package (H)

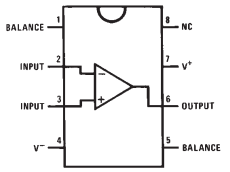


TL/H/5646–14

Order Number LF156AH, LF155H, LF156H, LF255H, LF256H, LF257H, LF355AH, LF356AH, LF357AH, LF356BH, LF355H, LF356H, LF357H, LM155AH/883, LM155H/883, LM156AH/883, LM156H/883, LM157AH/883 or LM157H/883*

See NS Package Number H08C

Dual-In-Line Package (M and N)



TL/H/5646–29

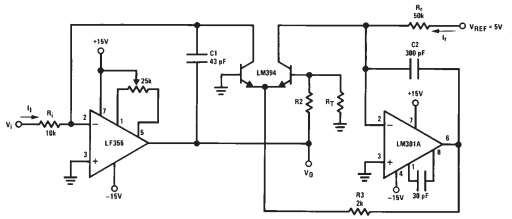
Order Number LF355M, LF356M, LF357M, LF355BM, LF356BM, LF355BN, LF356BN, LF357BN, LF355N, LF356N or LF357N

See NS Package Number M08A or N08E

*Available per JM38510/11401 or JM38510/11402

Typical Applications (Continued)

Fast Logarithmic Converter

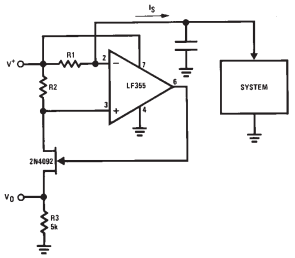


TL/H/5646–21

- Dynamic range: 100 μA ≤ I_i ≤ 1 mA (5 decades), $|V_O|$ = 1V/decade
- Transient response: 3 μs for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right]\frac{kT}{q} \ln V_i \left[\frac{R_r}{V_{REF}\, R_i}\right] = \log V_i \frac{1}{R_i I_r} R2 = 15.7k, R_T = 1k, 0.3\%/°C \text{ (for temperature compensation)}$$

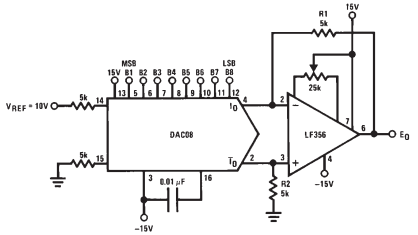
Precision Current Monitor



TL/H/5646–31

- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common-mode range to supply range
  - Low I_B
  - Low V_{OS}
  - Low Supply Current

8-Bit D/A Converter with Symmetrical Offset Binary Operation



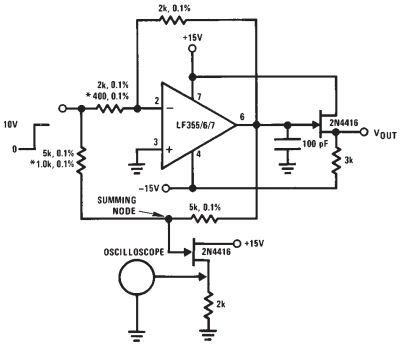
TL/H/5646–32

- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3 μs

E_O	B1	B2	B3	B4	B5	B6	B7	B8	Comments
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

Typical Applications

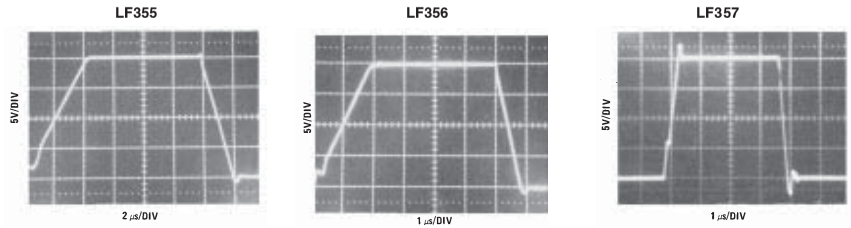
Settling Time Test Circuit



TL/H/5646–16

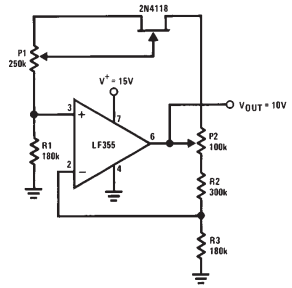
- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for A_V = −5
- FET used to isolate the probe capacitance
- Output = 10V step
- A_V = −5 for LF157

Large Signal inverter Output, V_{OUT} (from Settling Time Circuit)



TL/H/5646–17 TL/H/5646–18 TL/H/5646–19

Low Drift Adjustable Voltage Reference



TL/H/5646–20

- Δ $V_{OUT}/\Delta T$ = ±0.002%/°C
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
  - Low I_B
  - Low drift
  - Low supply current

LF155/LF156/LF157 Series Monolithic JFET Input Operational Amplifiers

Elektronik mit Steckbrett und Lötkolben

WS 2017/18

Prof. Dr. Eberhard Riedle

Lehrstuhl für BioMolekulare Optik
Fakultät für Physik, LMU München

What do we want to do ?

- In der Experimentalphysik spielt die **Instrumententwicklung** eine große Rolle. Auch wenn in einem Aufbau oft kommerzielle Module oder Komponenten zum Einsatz kommen, erfordert die logische Verschaltung durch Triggersignale und das schnelle Steuern und Regeln Grundkenntnisse in der elektronischen Signalverarbeitung. In vielen Fällen ist es auch zweckmäßig, kleine Schaltkreise (z.B. Filter) oder programmierbare Mikroprozessoren (z.B. Arduino) zu verwenden, um träge Softwarelosungen zu vermeiden. Weiterhin gibt es eine Reihe von wichtigen Messmethoden, insbesondere Lock in-Techniken, die weit verbreitet sind für die Auslese schwacher Signale in Gegenwart von Rauschen, die in den bisherigen Praktika aber leider nicht abgedeckt sind.

- Im Kurs wird der **Aufbau kleiner Schaltungen praktisch erprobt**. Vom einfachen Aufbau auf einem Steckbrett entwickeln wir uns zur gelöteten Platine bis hin zum Layout für geätzte Platinen. Zur Untersuchung der Schaltungen und zum Finden von Fehlern werden modernste **Oszillographen und Funktionsgeneratoren** verwendet.

- Ziel ist es, am Ende **eigene kleine Module aufzubauen**, die für spätere Praktikumsgruppen oder Forschungslabore funktionsfähig zur Verfügung stehen.

What does that really mean?

- Ich plane derzeit, das Praktikum an "Projekten" zu orientieren. Am Anfang müssen die Teilnehmer mal die **Messinstrumente** kennen lernen, gerade das **Picoscope** hat ja sehr viele Möglichkeiten. Hier werden wir verschiedene Wechselspannungsquellen mit passiven und aktiven Methoden überlagern.

- Danach planen wir einen Block zu **3-Weg-Lautsprechern**. Wir werden sowohl passive als auch aktive **Frequenzweiche**n bauen. Hier sehen Sie schon, dass nach oben viel Luft ist. Wer schon Erfahrung hat, kann sich ja an Tschebyscheff-Filtern höherer Ordnung versuchen, andere sind sicher mit etwas einfacheren ausgelastet.

- Als nächstes sollten wir etwas zu **Hochfrequenz** machen, da denken wir noch über die genauen Themen nach. Ein Beispiel, das ich gerade selbst bearbeite, ist ein Schmitt-Trigger mit wenigstens 100 MHz Bandbreite.

- Zum Ende würde ich gerne eine Schaltung entwickeln, mit der man **Hochleistungs-LEDs mit gewähltem Spitzenstrom und Pulslänge sowie Taktverhältnis betreibt**. Dabei kann man z.B. auch noch eine Leistungsstabilisierung mit optischer Detektion hinzufügen.

The real thing ….

Let‘s get started ….