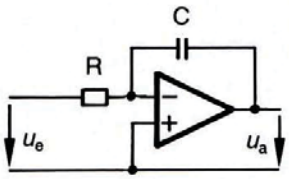
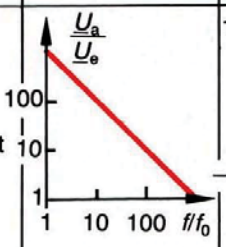
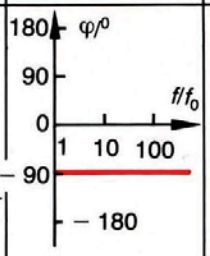
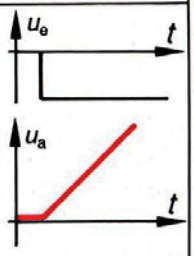
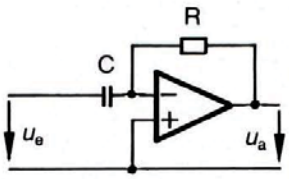
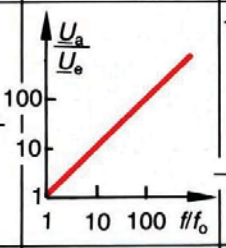
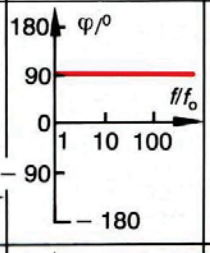
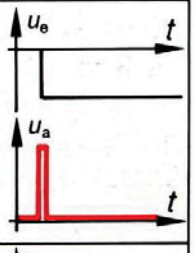
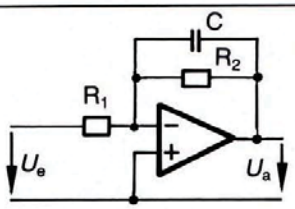
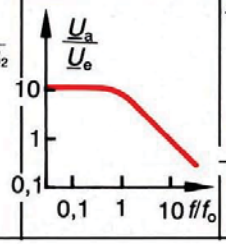
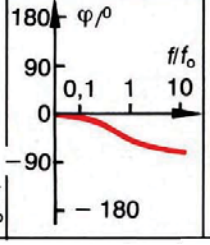
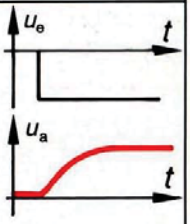
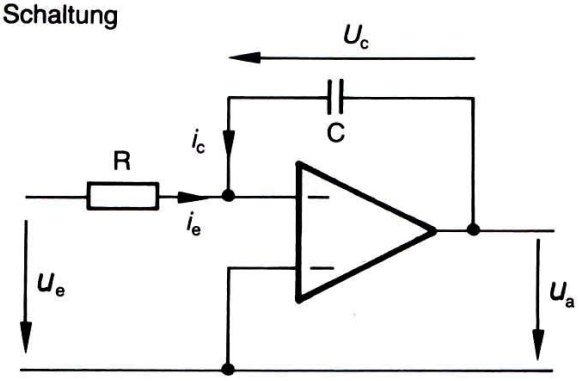
Dynamische Beschaltung des Operationsverstärkers

Schaltung	Eigenschaften Besonderheiten	Übertragungs-funktion $f = \underline{u}_a/\underline{u}_e$	Amplitudengang	Phasengang	Sprungantwort
	Integrator	$\underline{u}_a = -\frac{1}{RC}\int \underline{u}_e \, dt$			
	Differenzierer	$\underline{u}_a = -RC\frac{d\,u_e}{dt}$			
	Tiefpaß 1. Ordnung	$\frac{\underline{U}_a}{\underline{U}_e} = -\frac{R_2}{R_1}\cdot\frac{1}{1+j\omega CR_2}$ $\omega_g = \frac{1}{R_2C}$ $f_o = \frac{1}{2\pi R_2 C}$			

Integrator

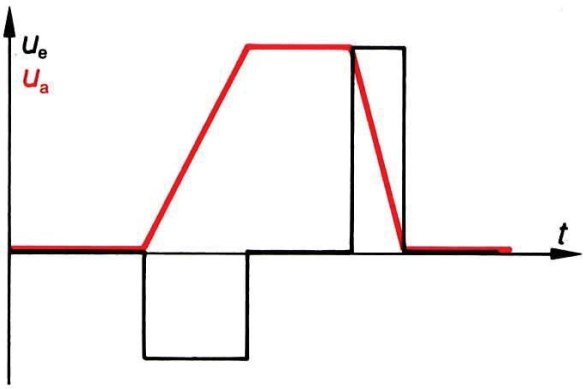
a) Schaltung



$$0 = i_e + i_C = \frac{u_e}{R} + C\frac{du_a}{dt} = 0$$

$$u_a = -\frac{1}{RC}\int u_e\,dt + U_C$$

b) Ein- und Ausgangsspannung



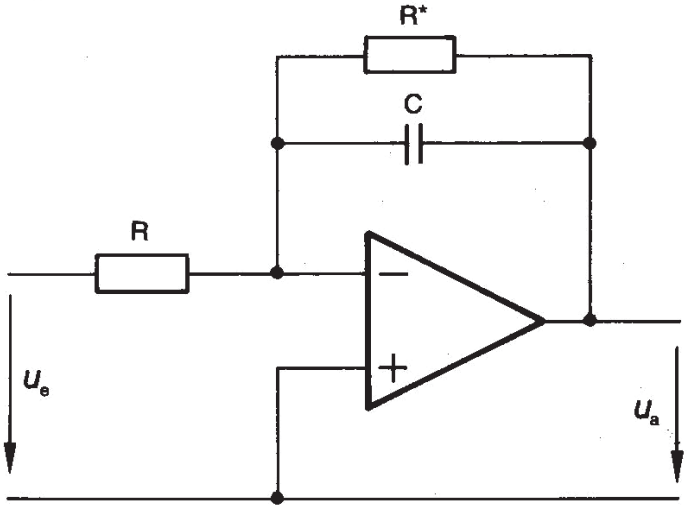
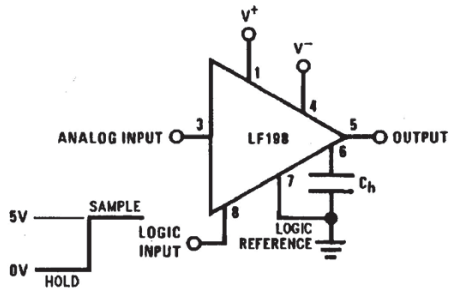
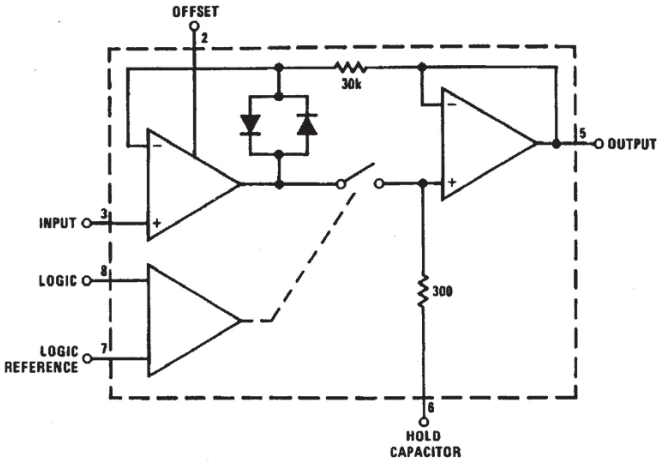


Bild 8-49. Integrator mit Gleichstrompfad.

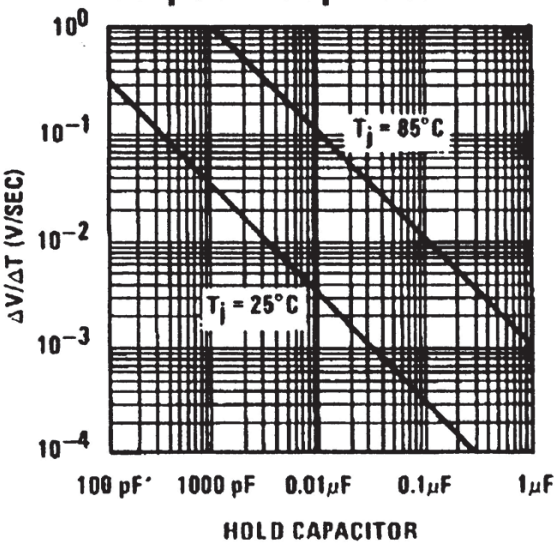
LF198/LF298/LF398, LF198A/LF398A
Monolithic Sample-and-Hold Circuits

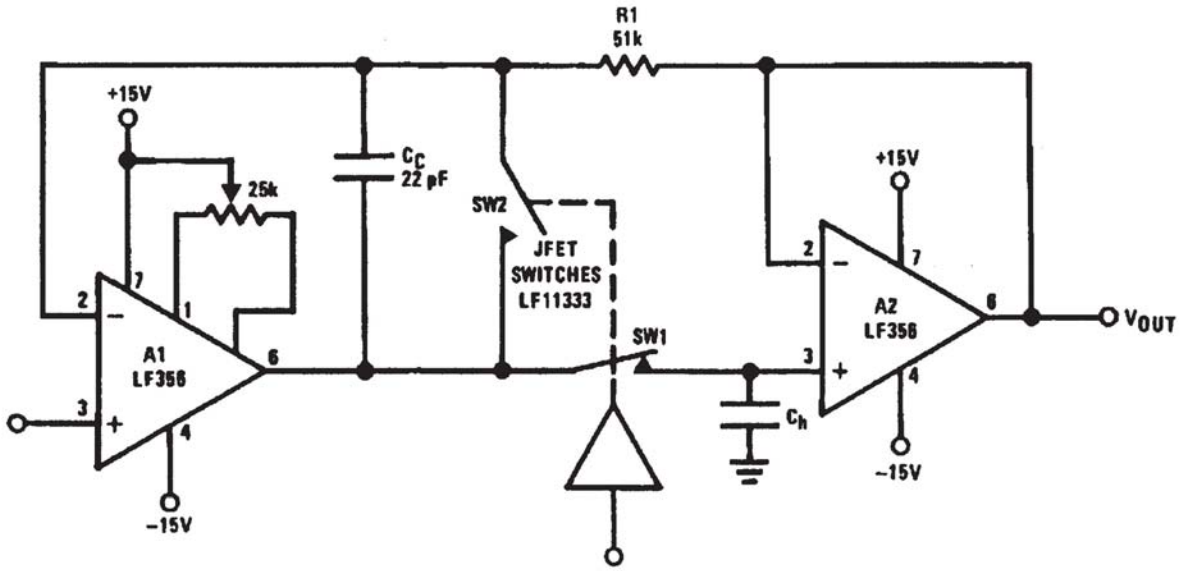


- Operates from ±5V to ±18V supplies
- Less than 10 μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at C_h = 0.01 μF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth
- Space qualified



Output Droop Rate

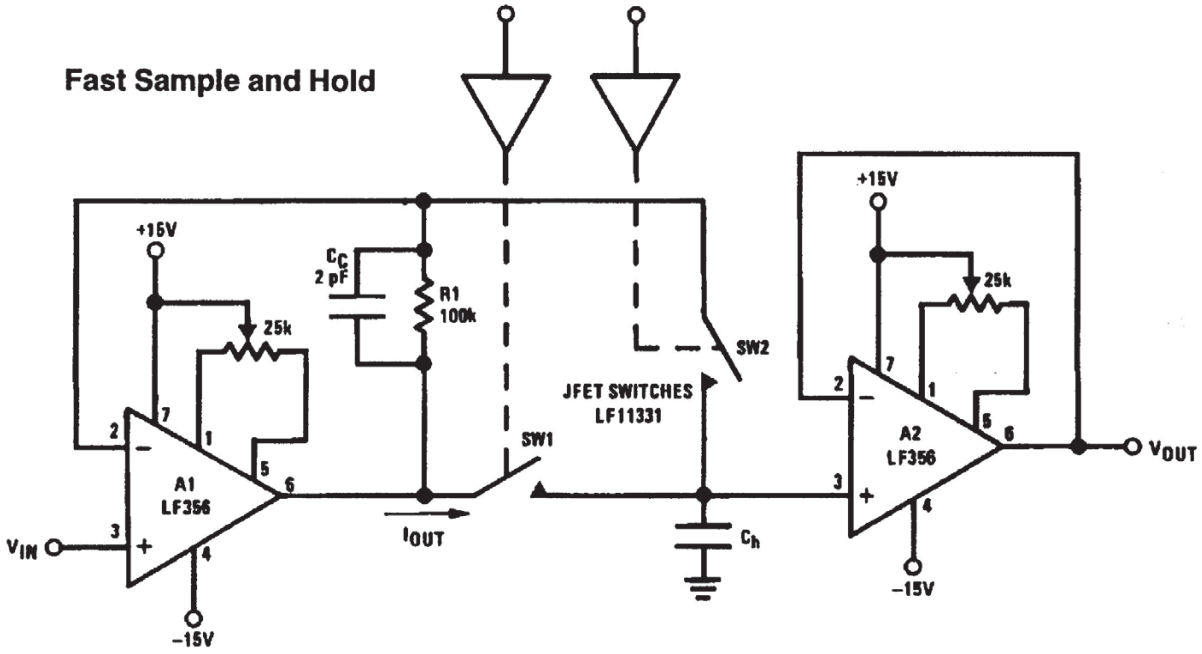




- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - Fast settling time
  - Low V_{OS}

High Accuracy Sample and Hold

Fast Sample and Hold

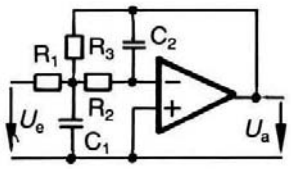
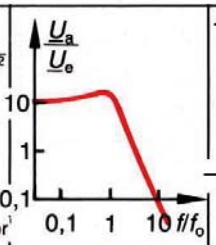
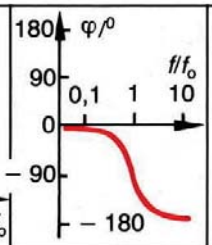
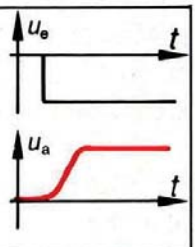
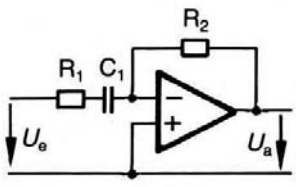
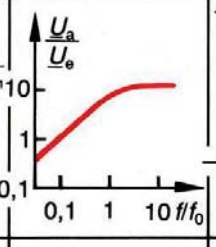
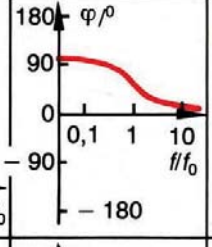
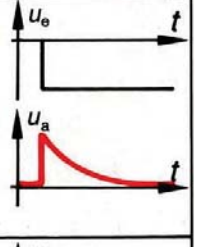
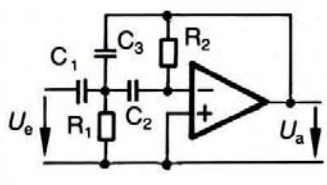
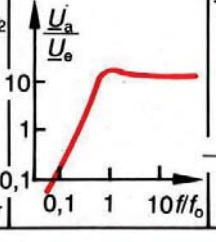
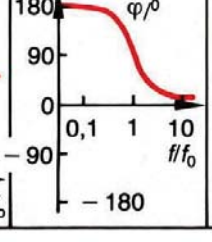
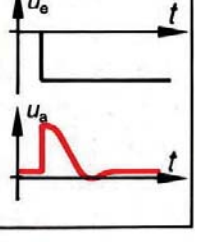


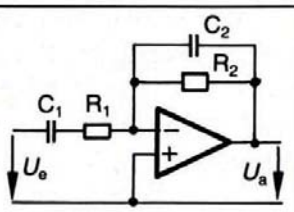
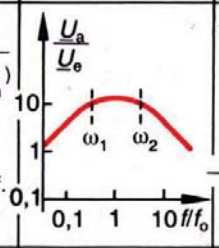
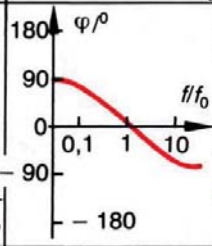
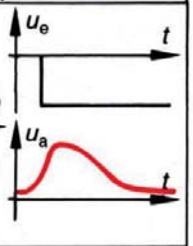
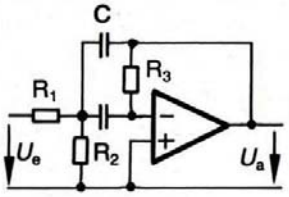
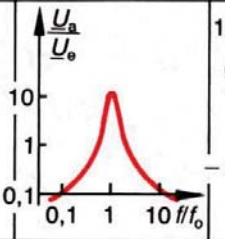
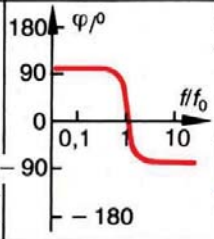
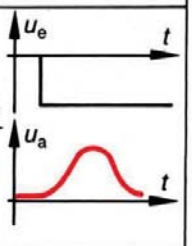
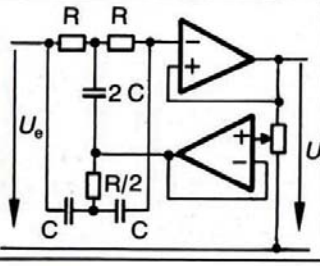
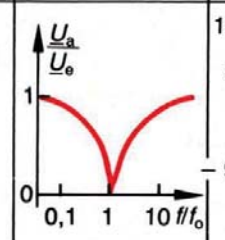
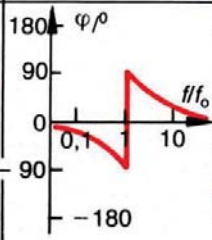
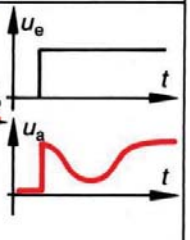
- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

$$T_A \cong \left[\frac{2R_{ON}, V_{IN}, C_h}{S_r}\right]^{1/2} \text{ provided that: } \quad V_{IN} < 2\pi S_r R_{ON} C_h \text{ and } T_A > \frac{V_{IN}\, C_h}{I_{OUT(MAX)}}, \; R_{ON} \text{ is of SW1}$$

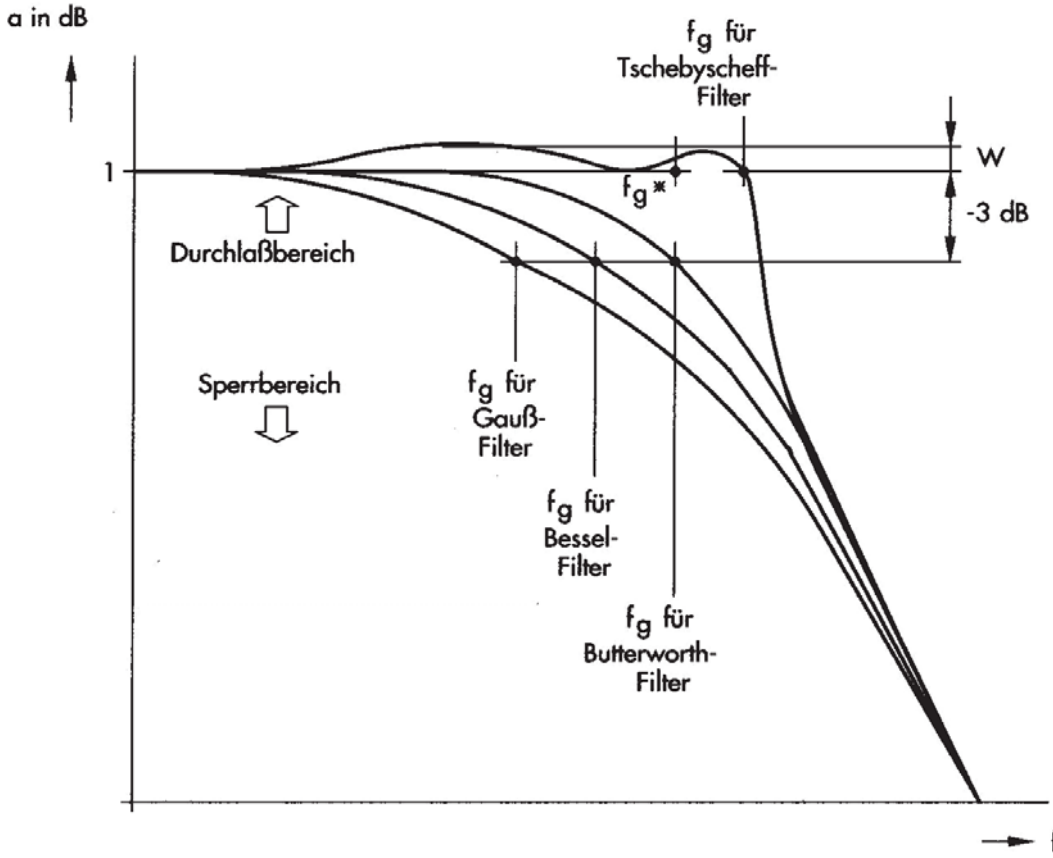
$$\text{If inequality not satisfied: } T_A \cong \frac{V_{IN}\, C_h}{20\ \text{mA}}$$

- LF156 develops full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

	Tiefpaß 2. Ordnung	$\frac{\underline{U}_a}{\underline{U}_e} = \frac{-V_0}{1+j\Omega\alpha-\Omega^2}$ $\Omega = \frac{\omega}{\omega_g}$ $V_0 = \frac{R_3}{R_1}$ α = Dämpfungsfaktor			
	Hochpaß 1. Ordnung	$\frac{\underline{U}_a}{\underline{U}_e} = -\frac{R_2}{R_1}\cdot\frac{j\omega C_1 R_1}{1+j\omega C_1 R_1}$ $\omega_o = \frac{1}{R_1 C}$			
	Hochpaß 2. Ordnung	$\frac{\underline{U}_a}{\underline{U}_e} = \frac{-V_\infty \Omega^2}{1+j\Omega\alpha-\Omega^2}$ $\Omega = \frac{\omega}{\omega_g}$ $V_\infty = \frac{C_1}{C_3}$ α = Dämpfungsfaktor			

Schaltung	Eigenschaften Besonderheiten	Übertragungs-funktion	Amplitudengang	Phasengang	Sprungantwort
	Bandpaß 1. Ordnung	$\frac{U_a}{U_e} = -\frac{R_2}{R_1} \frac{j\frac{\omega}{\omega_2}}{(1+j\frac{\omega}{\omega_2})(1+j\frac{\omega}{\omega_1})}$ $\omega_2 = \frac{1}{R_2C_2}$ obere Grenzf. (Tiefpaß) $\omega_1 = \frac{1}{R_1C_1}$ untere Grenzf. (Hochpaß)			
	Bandpaß 2. Ordnung	$\frac{U_a}{U_e} = V_0 \frac{j\frac{\Omega}{Q}}{1-\Omega^2+j\frac{\Omega}{Q}}$ $\Omega = \frac{\omega}{\omega_g}$ Q = Güte			
	Bandsperre mit Notch-Filter	$\frac{U_a}{U_e} = \frac{-V\Omega^2}{1-\Omega^2+(1-a)4j\Omega}$ $\Omega = \frac{\omega}{\omega_0}$ $\omega_o = \frac{1}{RC}$			

Aktive Filter mit optimierten Eigenschaften



- Tschebyscheff
- Gauss
- Bessel
- Butterworth

Bestimmung der Eigenschaften durch Wahl der Beschaltungspa-rameter entspre-chend Tabellen.

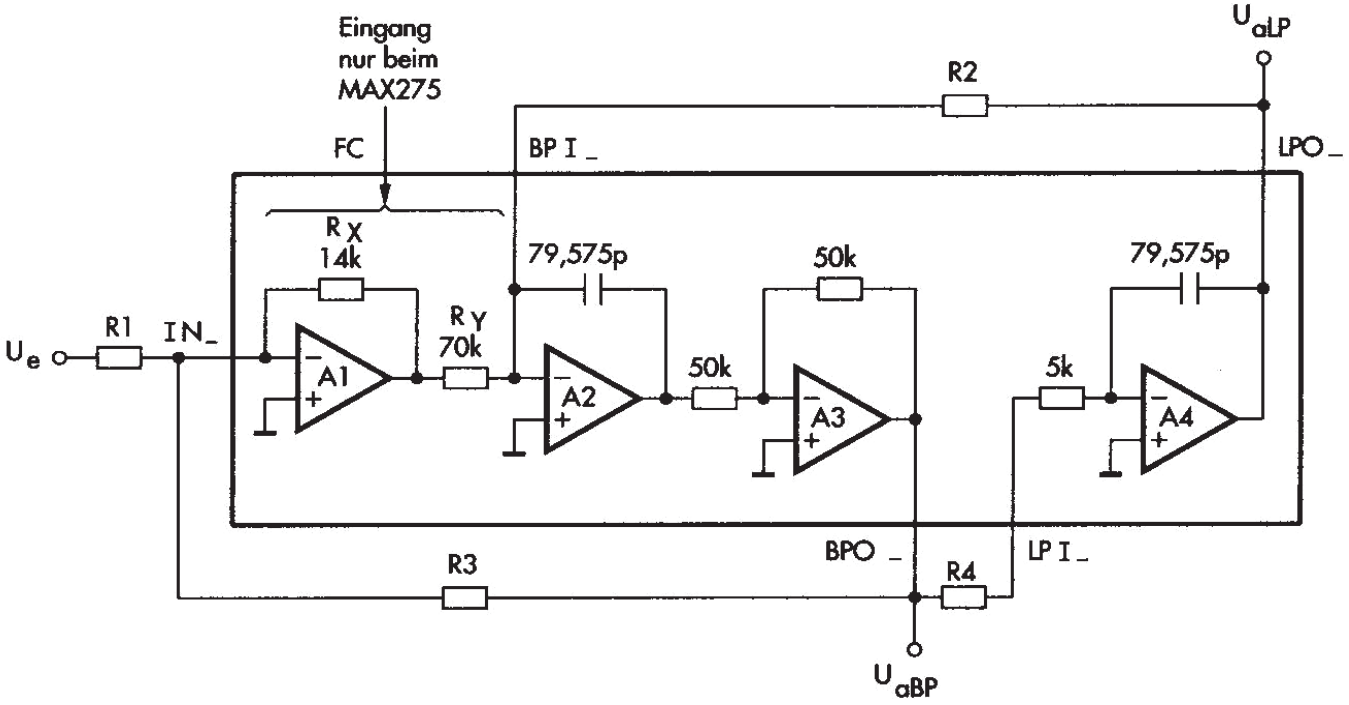
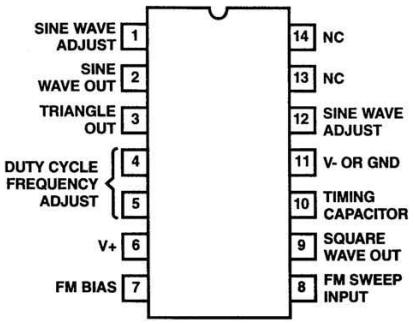


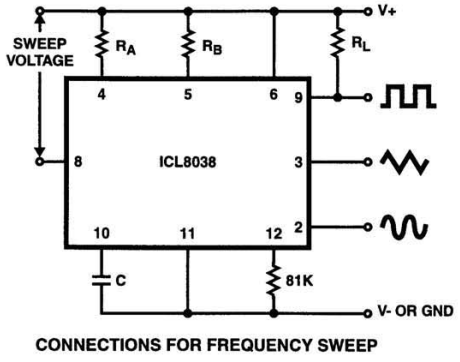
Abb. 5.37: Aufbau einer kontinuierlichen Filtersektion in den MAX-Bausteinen

HARRIS Semiconductor

ICL8038

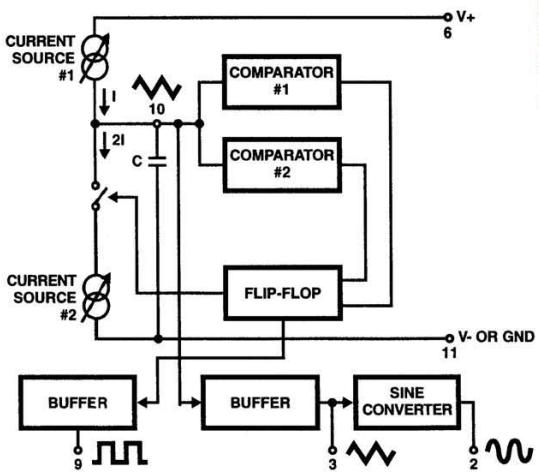
Precision Waveform Generator/Voltage Controlled Oscillator

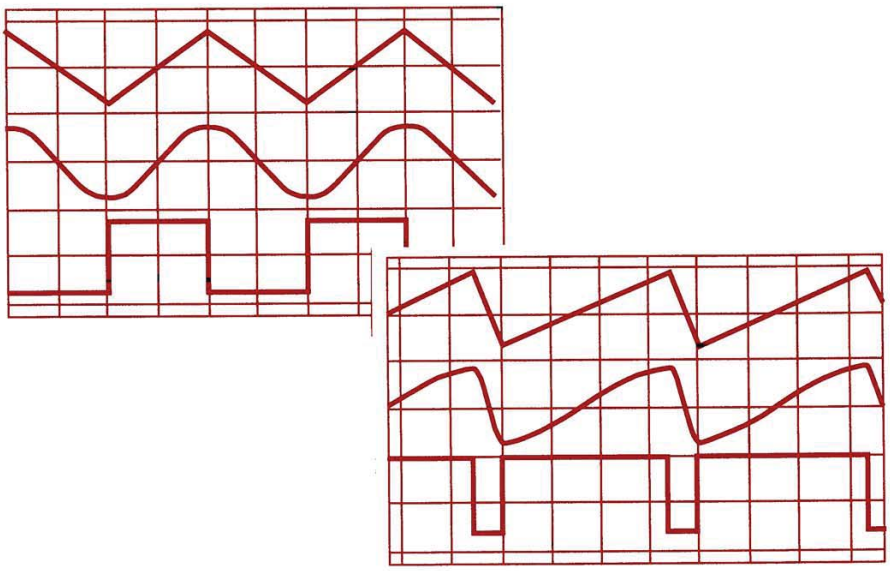




CONNECTIONS FOR FREQUENCY SWEEP

Functional Diagram





Programmable Frequency Scan Waveform Generator

AD5932

FUNCTIONAL BLOCK DIAGRAM

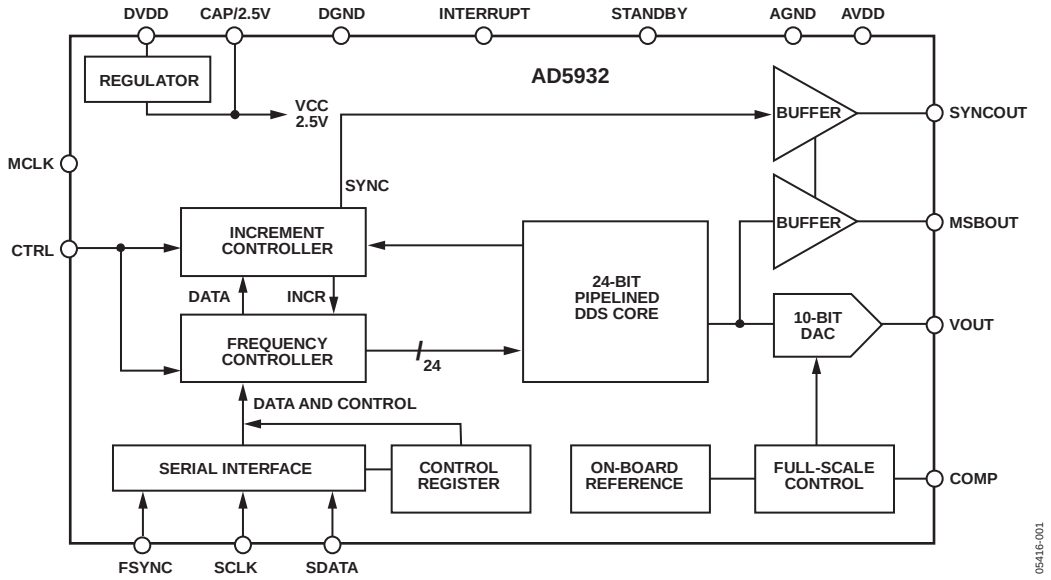
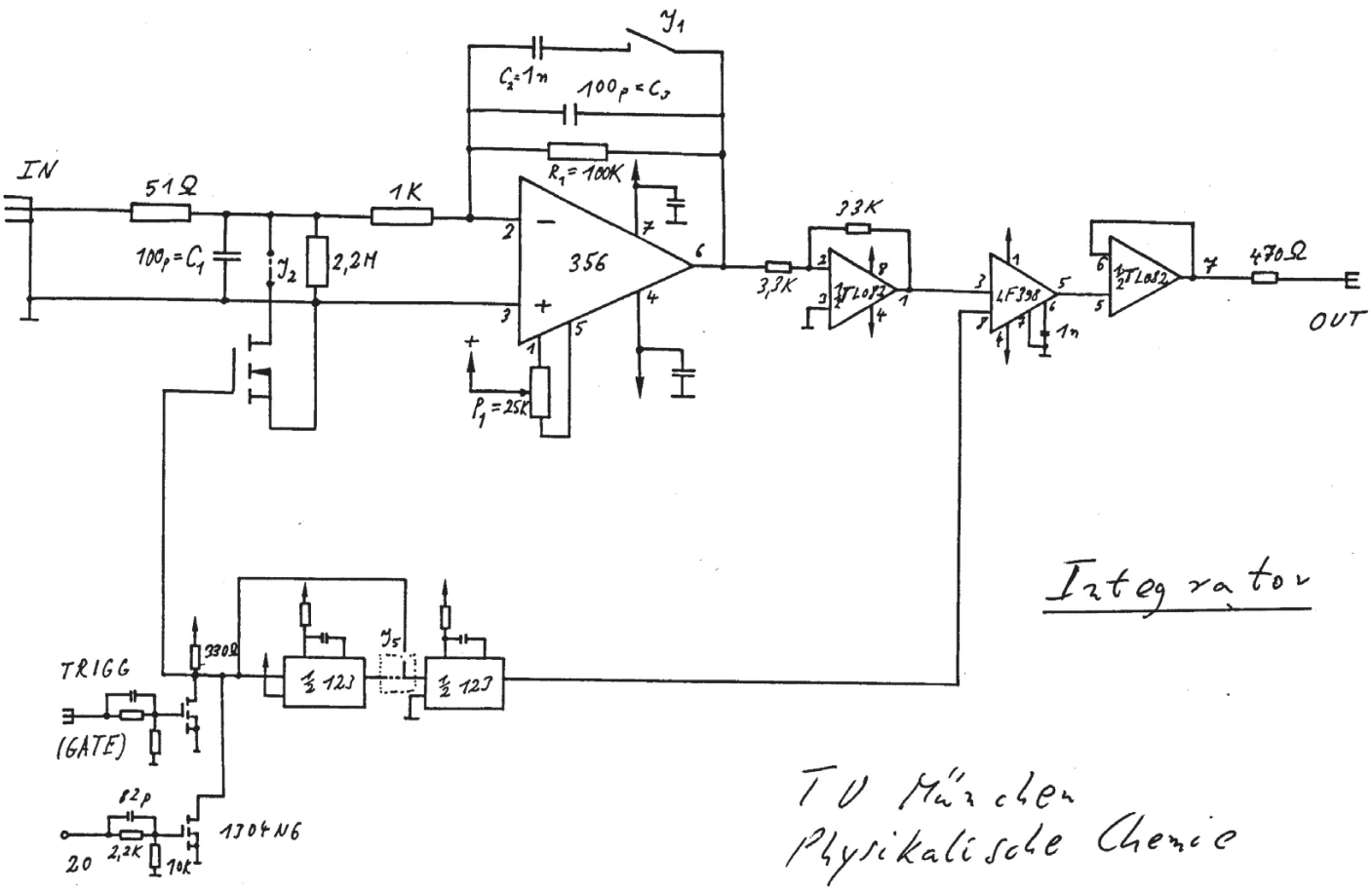


Figure 1.



Integrator

TU München, Physikalische Chemie

Documentation: E. Riedle, July 1990

The simple circuitry is intended for integration of current signals in pulsed laser experiments. **It is not a gated integrator**, however, there is a trigger (gate) input for suppression of dc signals present in the detector and triggering of the sample-and-hold amplifier. Typical applications are determination of the (relative) pulse energy, recording of an I_2 absorption spectrum or tracking of a SHG crystal.

Description:

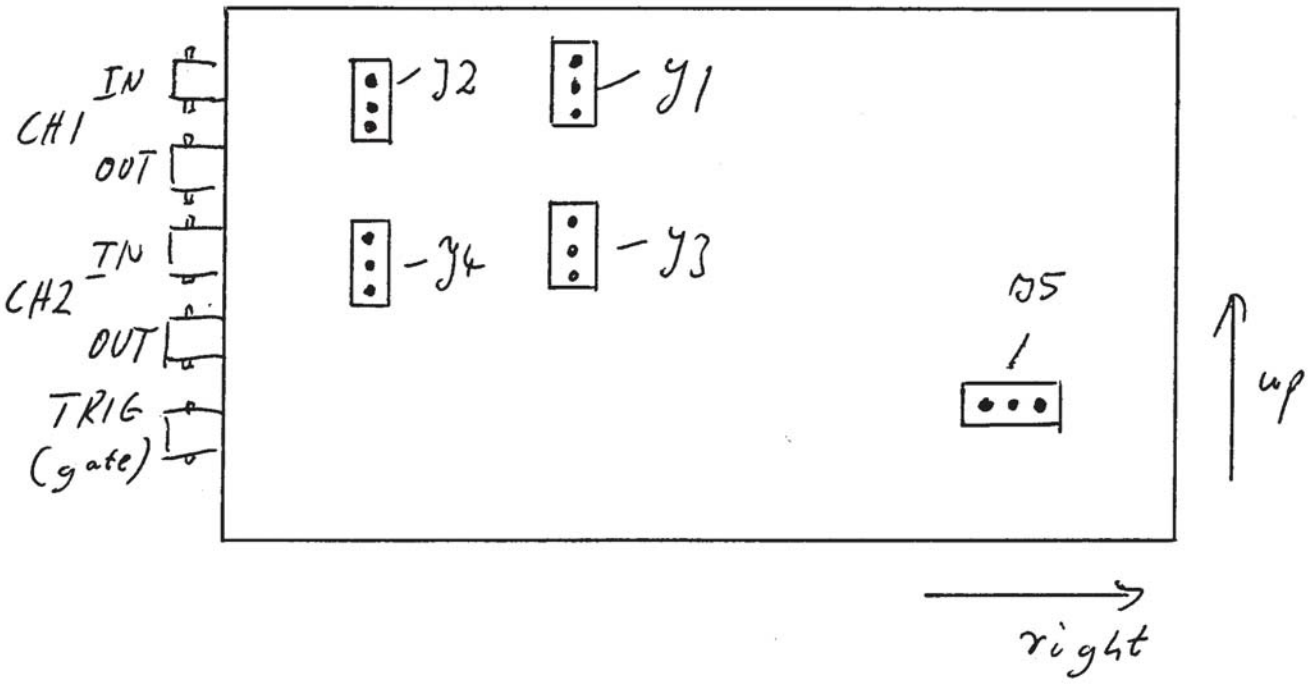
The incoming current signal (e.g. from a photodiode) is integrated in the capacitor C_1. This happens very fast, the termination of the detector (and its time response) is effectively given by the 51 Ω resistor (at input). Next, the charge stored in C_1 is transfered by the op-amp "356" to the capacitor C_2 and/or C_3 on a µs timescale. The resulting output voltage is amplified by x 10 in the "1/2 TL082" amplifier and finally held constant for long times by the "LF398" sample-and-hold amplifier. The second "1/2 TL082" is used as an output buffer.

To clear the C_2/C_3 capacitor before the next laser pulse, a 100 KΩ resistor is added on the "356" amplifier. This discharge takes on the order of milliseconds. To avoid strong influence from dc leakage currents in the detector, the capacitor C_1 is shortened for most of the time by a FET. To activate the integrator around the appearance time of the desired signal, a positive pulse should be applied at the trigger/gate input from 0.5 µs before the actual signal to about 5 - 15 µs after the end of the signal. **This is not intended for selection of part of the signal, like in a gated integrator.** The end of the trigger pulse triggers the sample-and-hold amplifier with some additional internal delay.

The sensitivity of the integrator is 10 V output for an input signal of 50 ns·V in 50 Ω termination if C_2+C_3 are used, and tenfold higher for only C_3. The input signal should be set with a fast osciloscope (50 Ω termination) for appropriate levels.

Front panel plugs and controls:

There are two BNC plugs for input and output of each channel. For each channel there is also a potentiometer (P_1) to set the zero point. These can also be used to suppress a small offset. The trigger/gate signal can either be applied at the front BNC plug or the no. 20 pin on the back conector.



Jumpers on the pc-board:

On each plug-in unit, there are two integrator channels and one common triggering unit. There are 5 jumpers located on the board which are used as follows:

J1: Sensitivity of CH1. In the upper postion the capacitors C_2 and C_3 are used in parallel to decrease sensitivty and temperature drift. In the lower position only C_3 is active.

J2: In the lower postion the FET is activated to shorten the capacitor C_1 between laser pulses (see above). In the lower position the FET is not active and the input signal will be applied for all times.

J3: Like J1 for CH2

J4: Like J2 for CH2

J5: In the right position additional internal delay for the sample-and-hold is used. In the left position there is no additional delay.