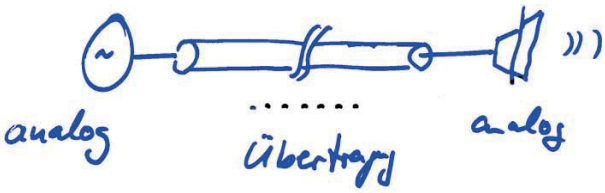
Digital-Analog-Konverter (DAC)

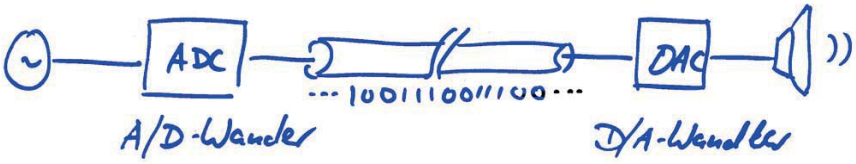
Problem: geringe Abweichung der Übertragungselemente von der Idealität führt durch Fehlerfortpflanzung zu großem Fehler

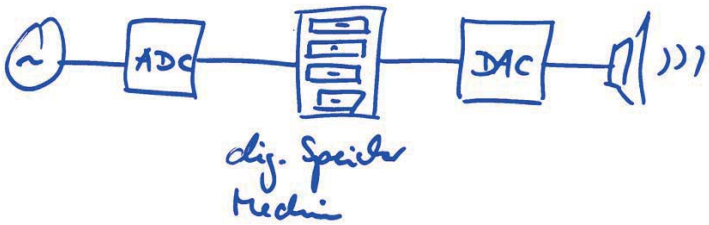


analoge Technik: **Minimierung** der Fehler

digitale Technik: **Verhinderung** der Fehler

"bessere" Lösung:



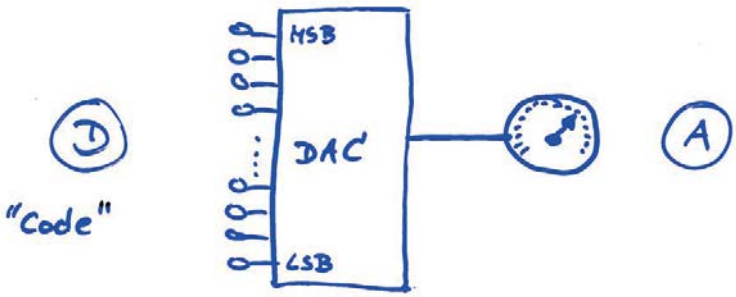


Große Vorteile auch bei der Speicherung analoger Daten !

Forderungen an Wandler:

1) "Genauigkeit" steigt prinzipiell mit Abtastrate → **schnell**
2) "Genauigkeit" steigt prinzipiell mit der Auflösung → **"breite" Worte**
3) "Genauigkeit" wird besser, wenn Fehlertolerant → **Fehleranalyse, Software**
   → **"breite" Worte**

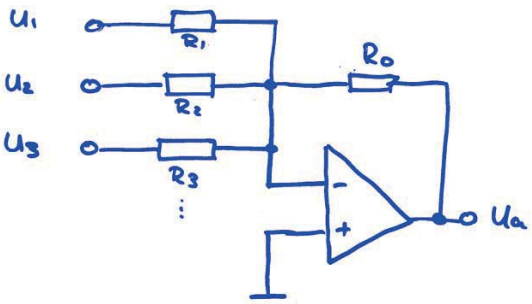
Problem:



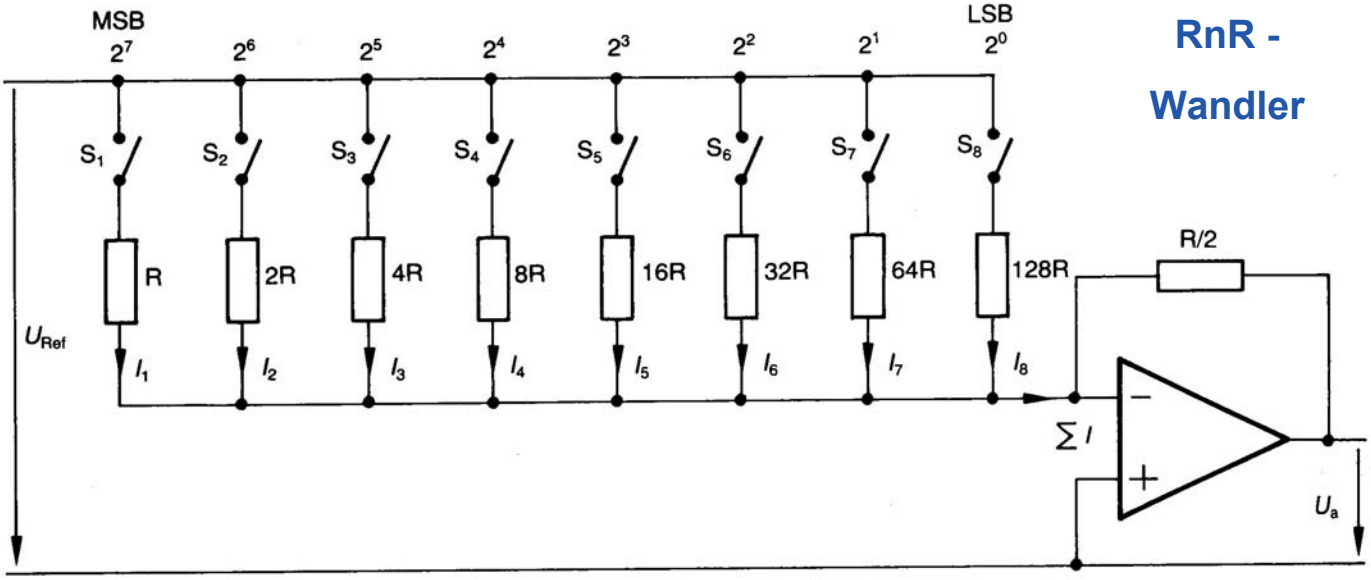
Forderung: Digitalwort ∝ Analogsignal

Grundprinzip:

Analogaddierer



$$\frac{U_1}{R_1}+\frac{U_2}{R_2}+....+\frac{U_n}{R_n}=-\frac{U_a}{R_o}$$



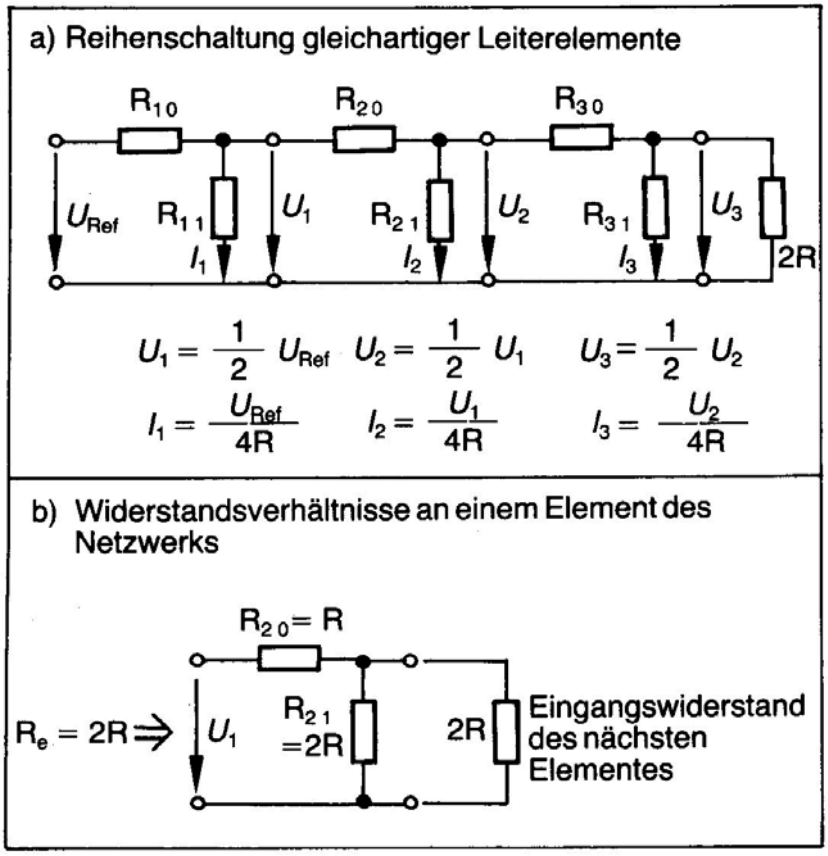
RnR - Wandler

Beim RnR-Wandler müssen viele verschiedene Widerstände mit sehr unterschiedlichem Wert verwendet werden. Dies führt zu Problemen bei der Präzision.

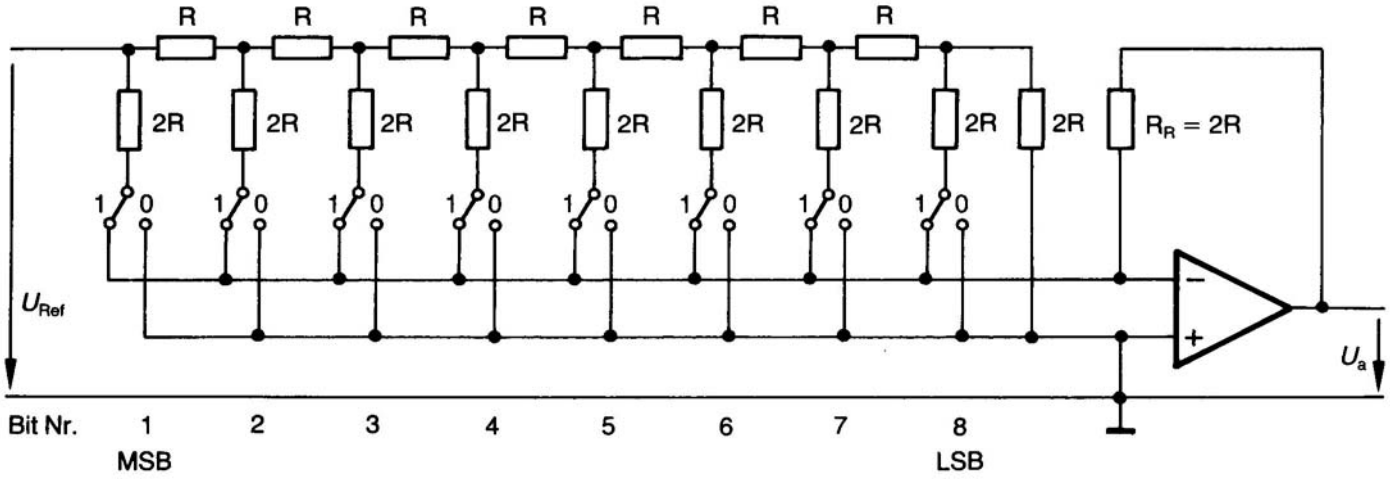
Durch die Verwendung eines **R2R-Netzwerkes** aus Widerständen mit nur 2 unterschiedlichen Werten kann dieses Problem vermieden werden.

Damit läßt sich ein sehr präziser **R2R-Wandler** bauen.

http://ac16.uni-paderborn.de/arbeitsgebiete/messtech/simulationen/da/index.html

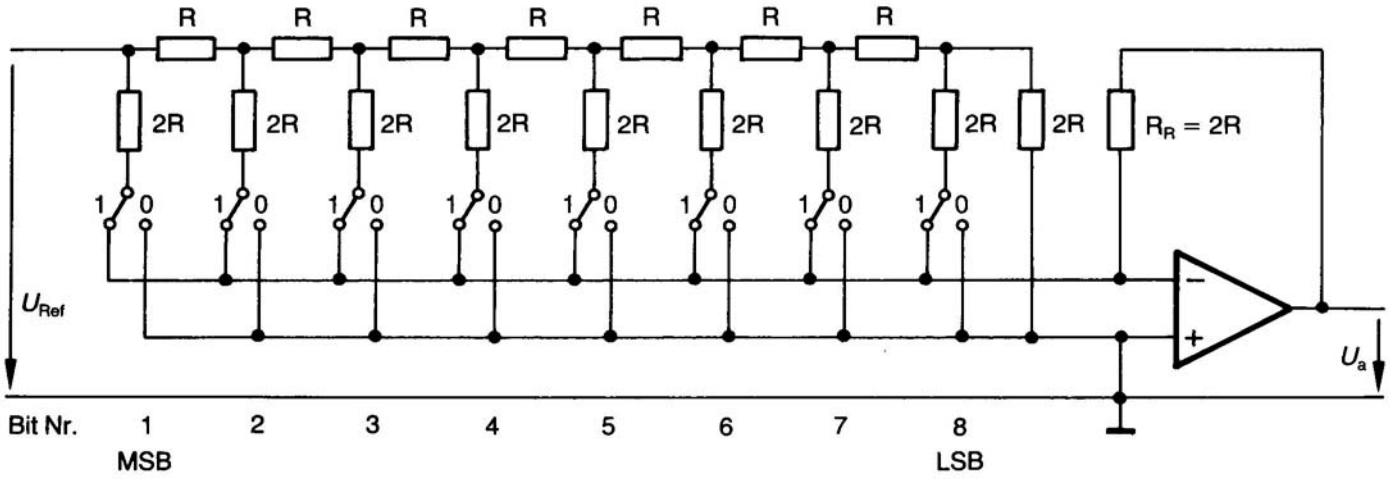


R2R - Wandler



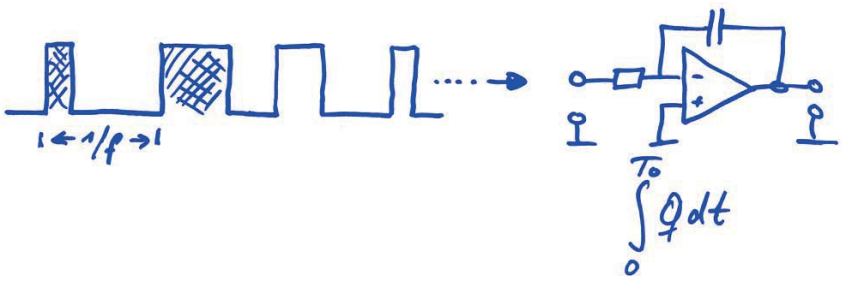
Wie groß ist der Eingangswiderstand und
wie hängt er von der Anzahl der Stufen ab?

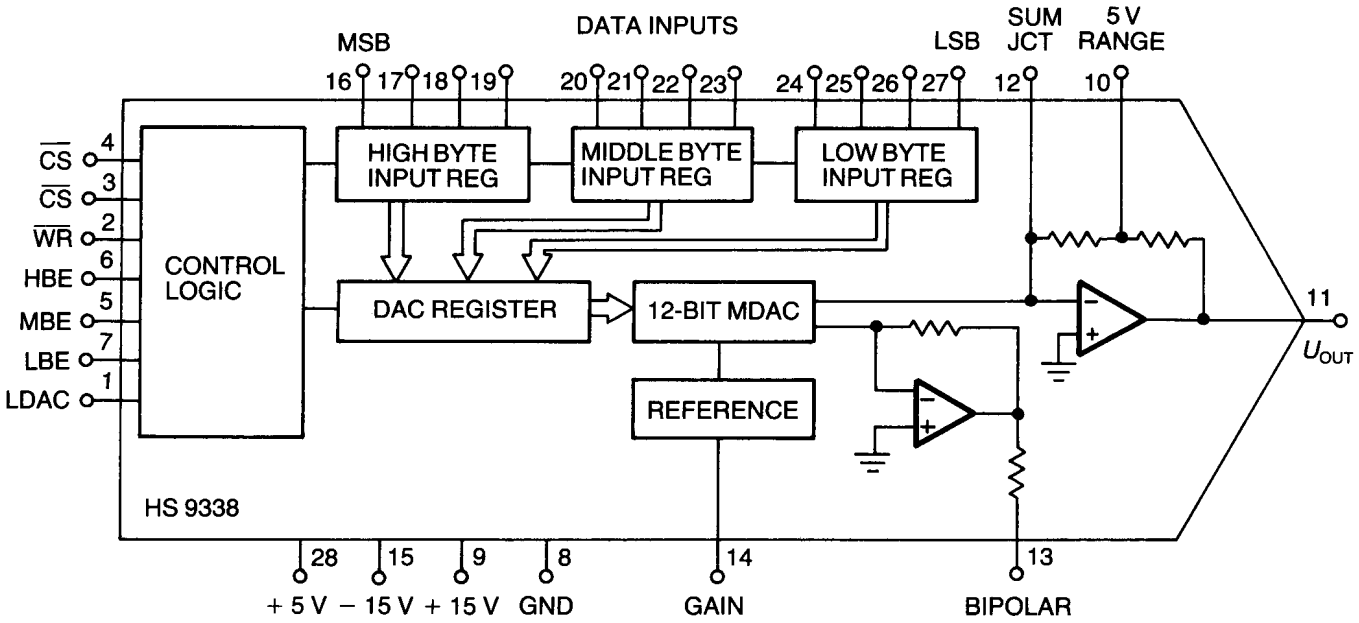
R2R - Wandler



Weitere Möglichkeit:

Pulsbreiten-Konverter





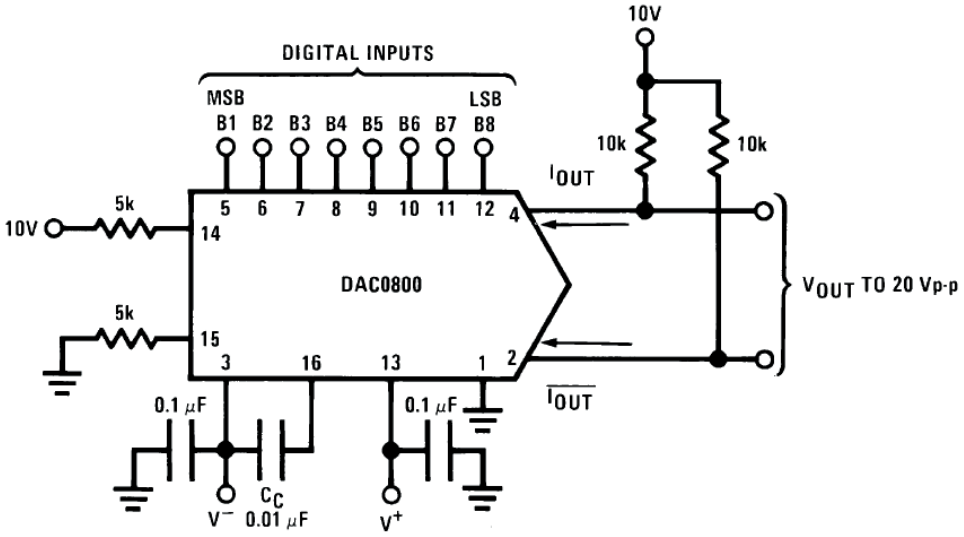
Digital-Analog-Wandler mit Mikroprozessor-Schnittstelle.

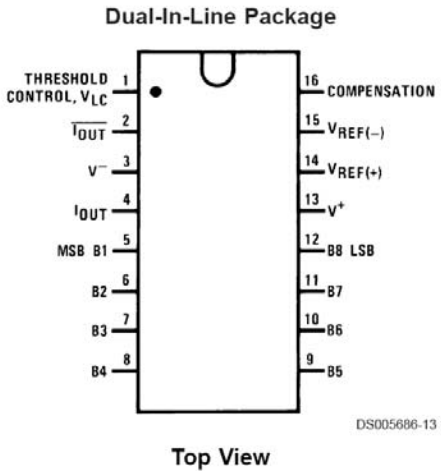
Features

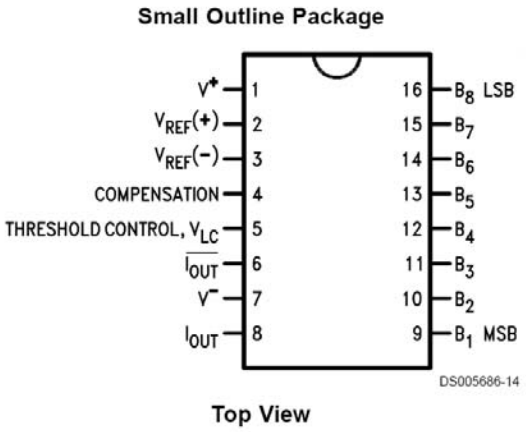
- Fast settling output current: 100 ns
- Full scale error: ±1 LSB
- Nonlinearity over temperature: ±0.1%
- Full scale current drift: ±10 ppm/°C
- High output compliance: −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range: ±4.5V to ±18V
- Low power consumption: 33 mW at ±5V
- Low cost

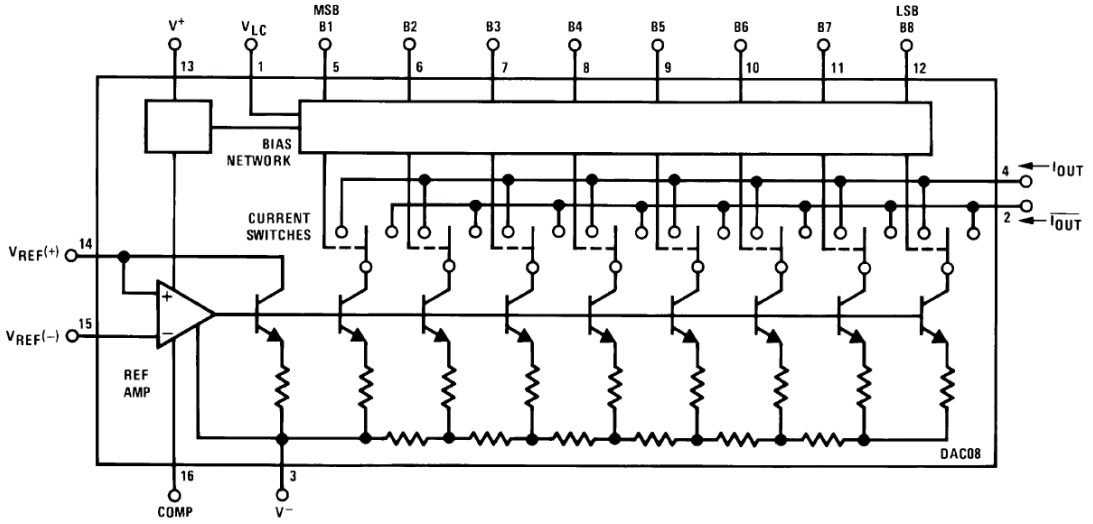
National Semiconductor

DAC0800/DAC0802
8-Bit Digital-to-Analog Converters



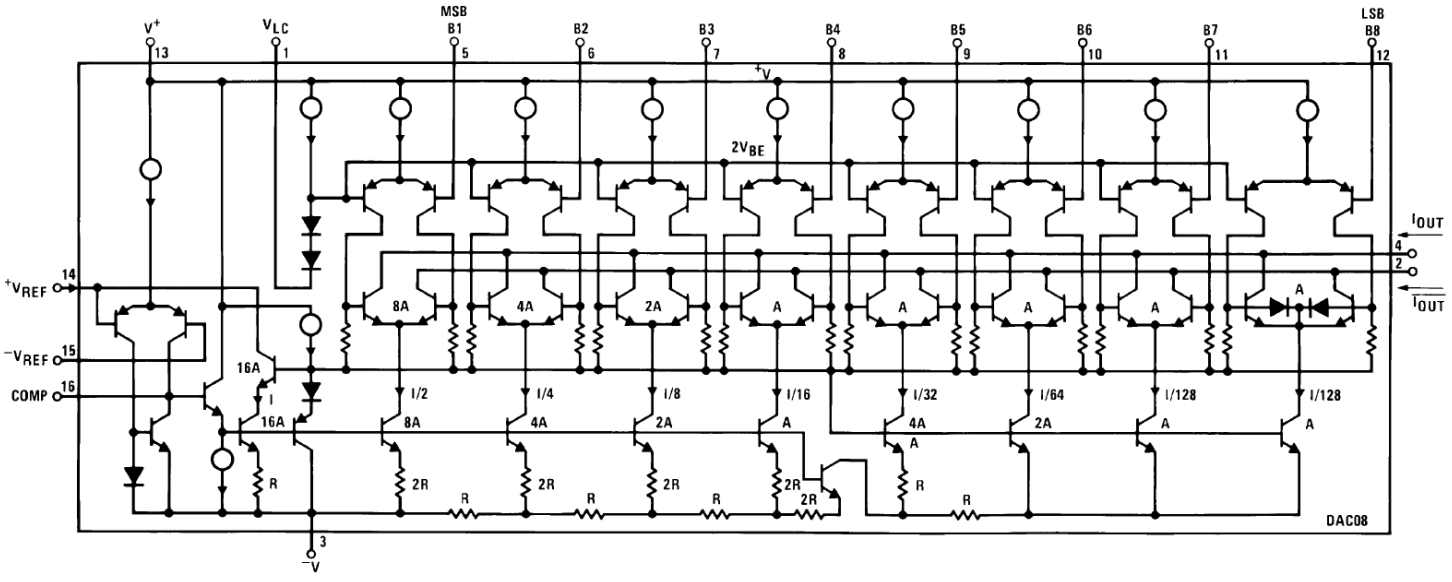




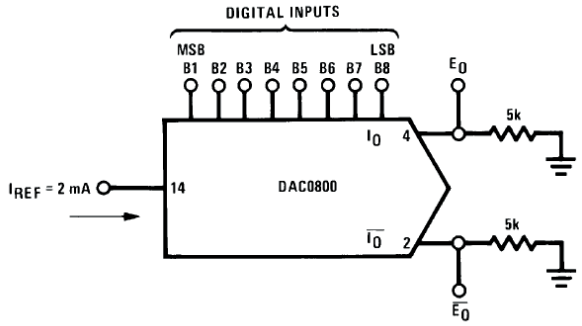


k LMU

Equivalent Circuit

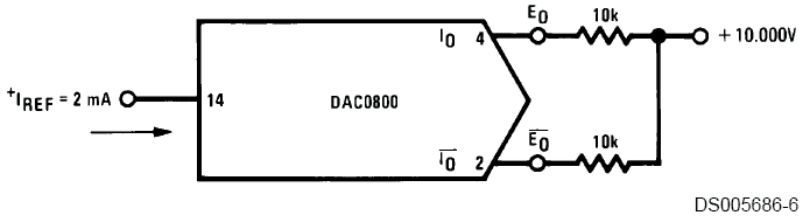


DS005686-15



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I}_O$mA	E_O	$\overline{E}_O$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full Scale−LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half Scale+LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half Scale−LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero Scale+LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

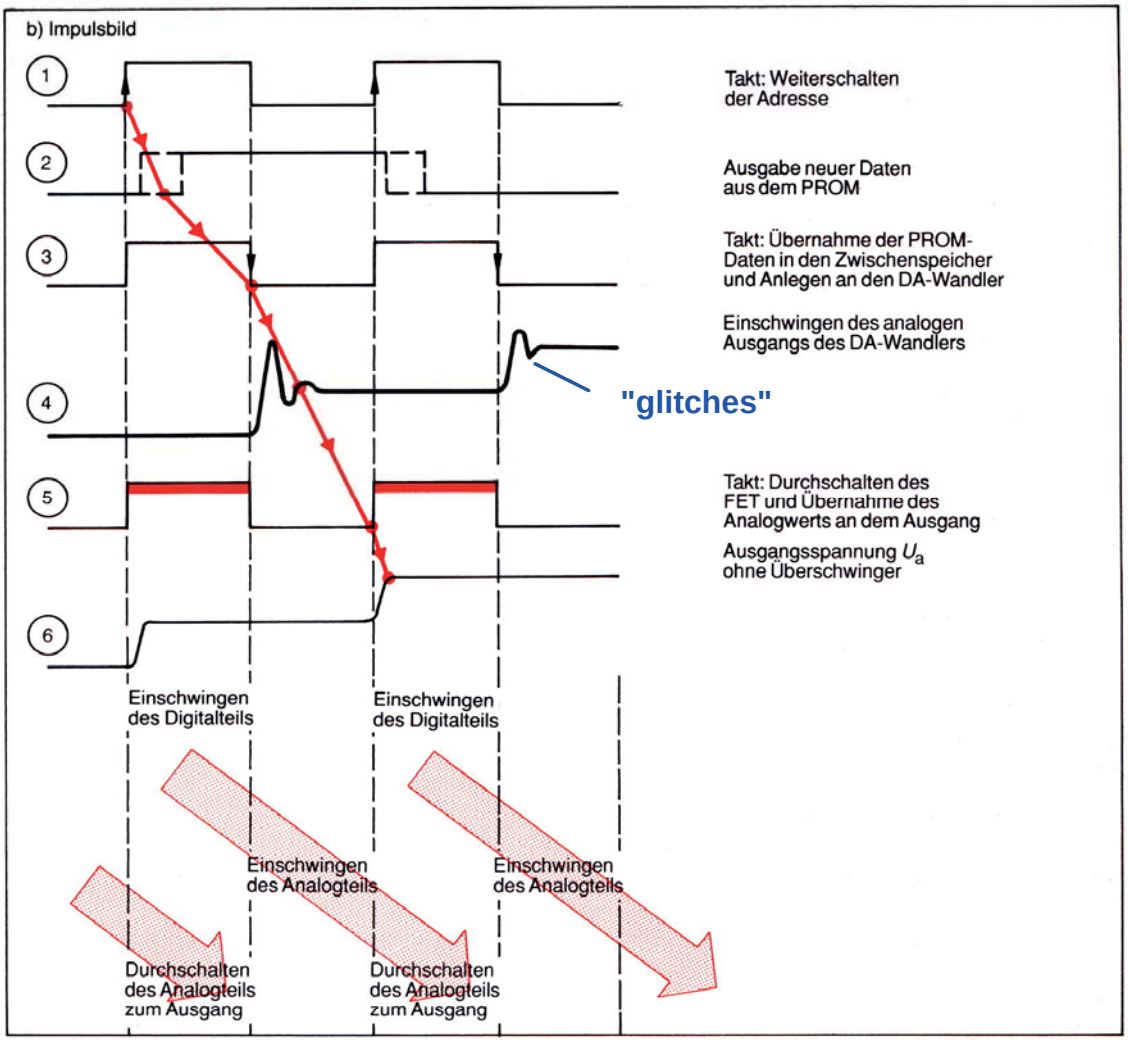
FIGURE 6. Basic Unipolar Negative Operation (Note 5)



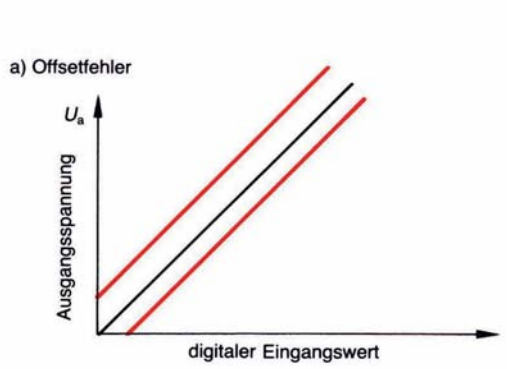
	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E}_O$
Pos. Full Scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero Scale+LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale−LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	−9.920

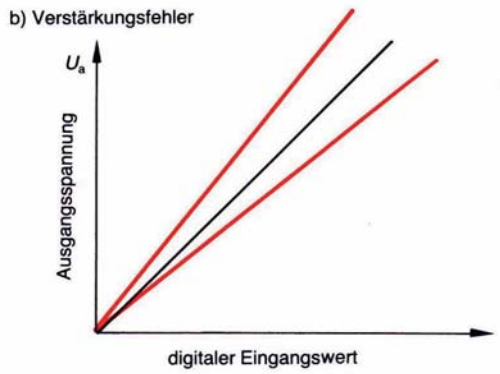
FIGURE 7. Basic Bipolar Output Operation (Note 5)

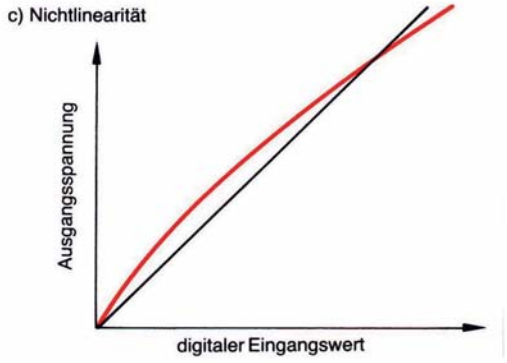
Digitaler Funktions-generator

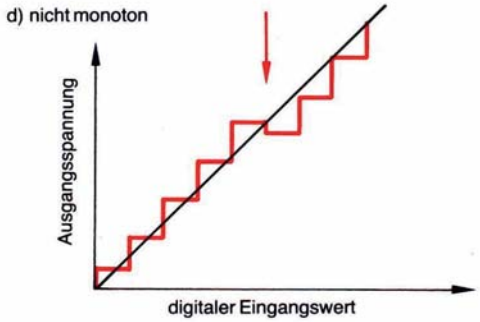


Fehler bei Datenwandlern










OFF
1000
750
200
20
2000
200
2000
200
20K
2000
200
10A
10A MAX
VC 301
VOLTCRAFT®
MULTIMETER
VΩmA
1000V DC
750V AC
200mA MAX
500V MAX
COM


ICL7106CPL
H9527
SUPER
ALKALINE

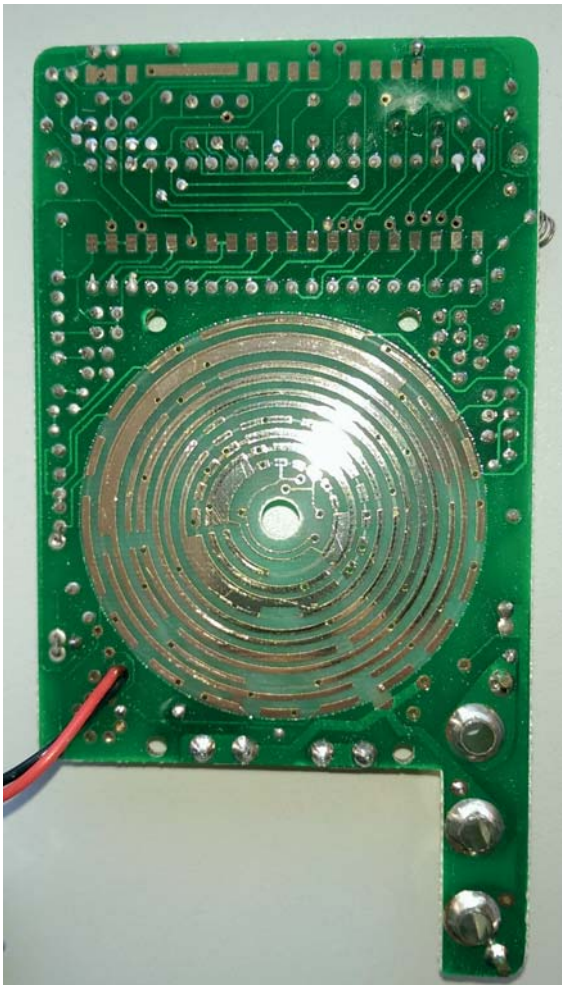
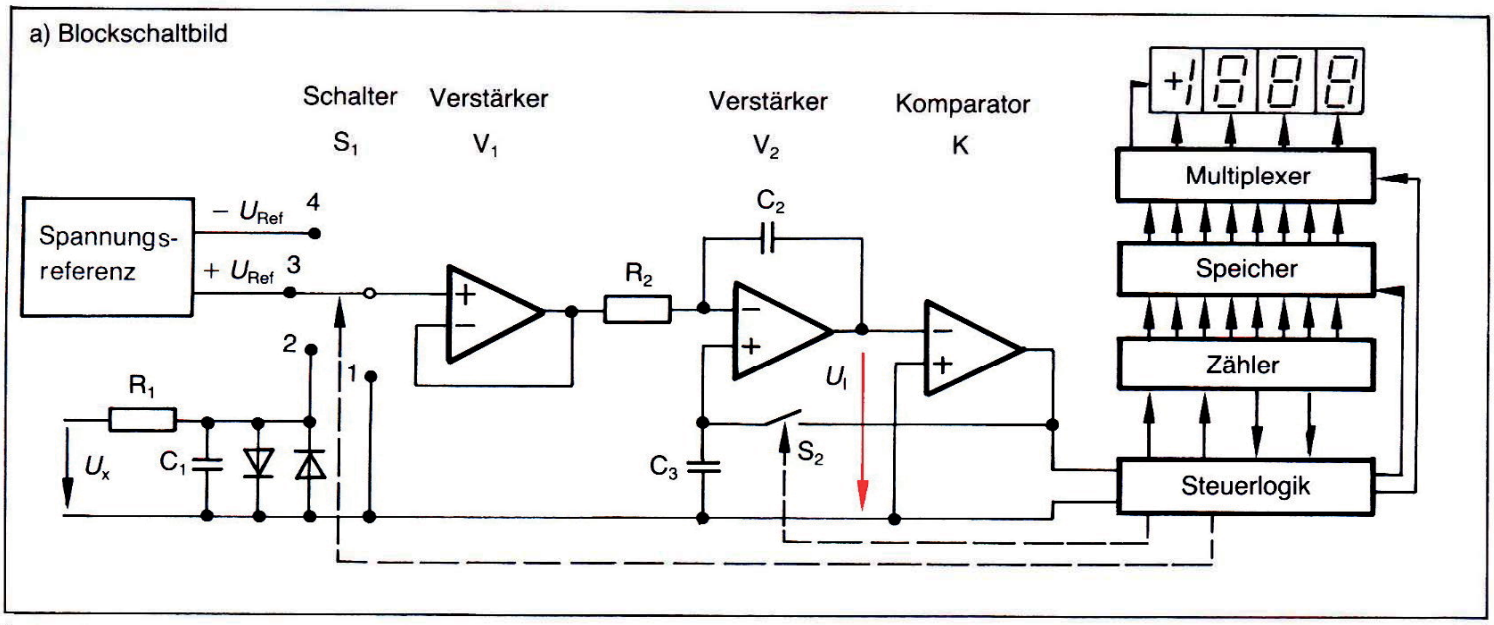
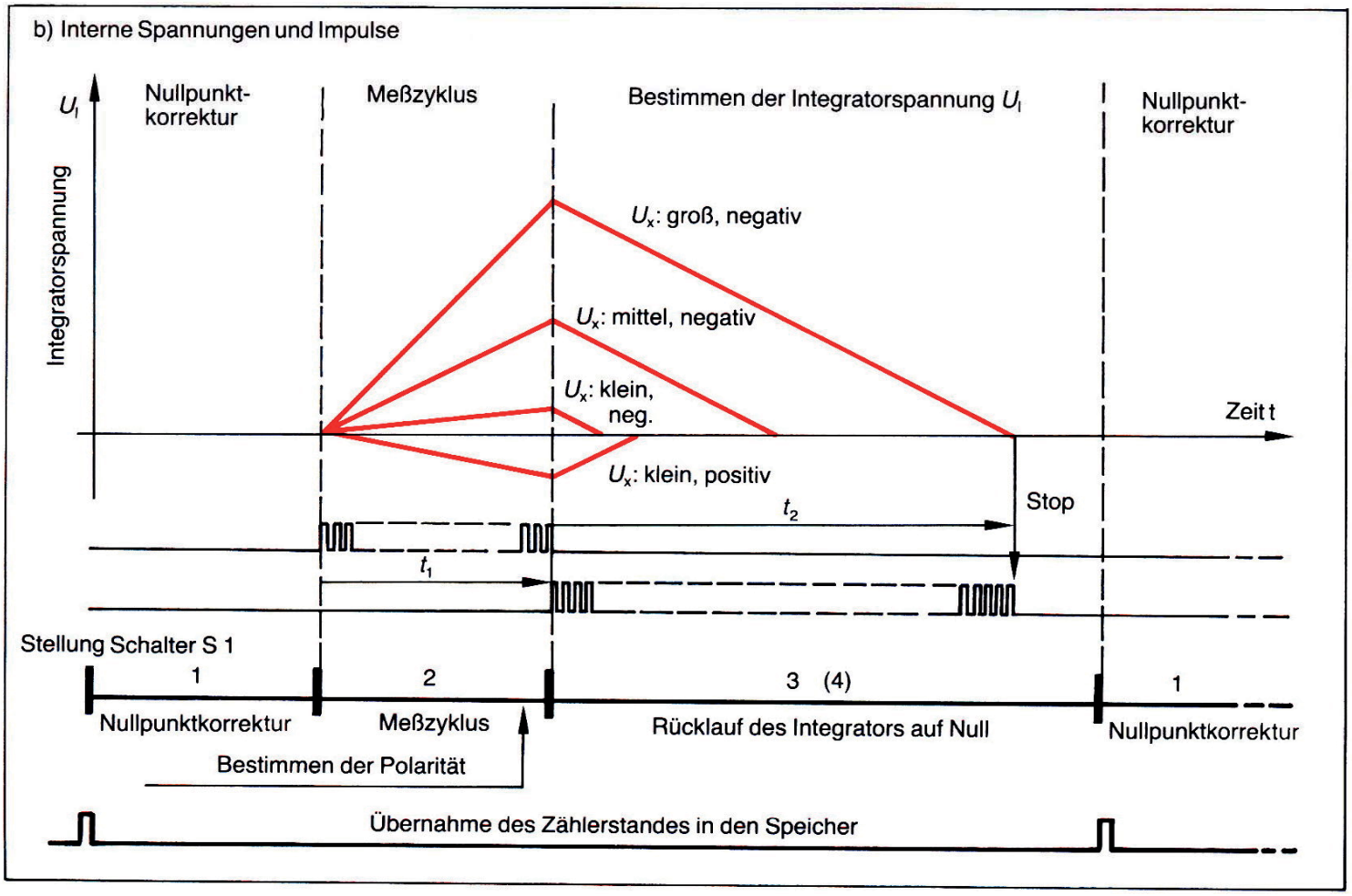


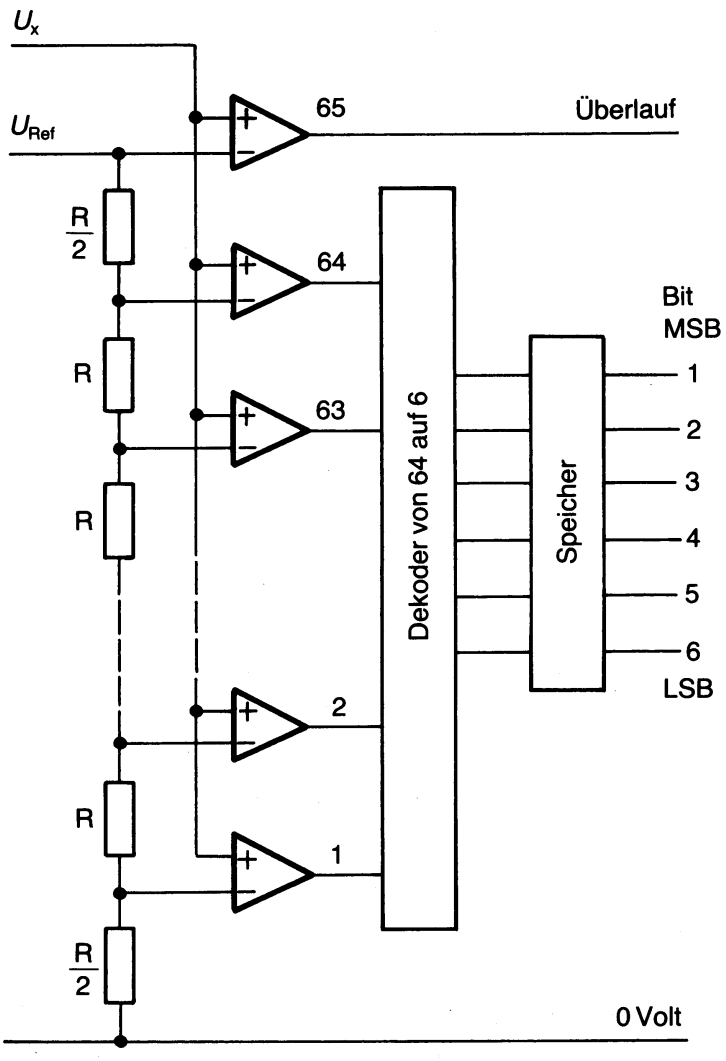
Tabelle 9-1. Verfahren zur Analog-Digital-Wandlung.

Arbeitsprinzip	Genauigkeit, Schnelligkeit	Preis, Stromverbrauch	Ausgang	Anwendungsbeispiel
integrierender AD-Wandler, Zweirampenverfahren	dezimal: 3½ bis 5½ Stellen binär: 12 bis 20 Bit, 10 ms bis 1 s, langsam	sehr preisgünstig, 1 mW bis 100 mW	BCD mit Ziffernanzeige, binär, parallel, µP-kompatible Busschnittstelle	Digitalmultimeter, langsame Spannungsmesser, für manuelle und automatische Messungen; unempfindlich gegen überlagerte Störungen
AD-Wandler nach dem Prinzip der sukzessiven Approximation	binär, 8 bis 18 Bit, 0,5 µs bis 100 µs, schnell	preisgünstig bis mittlere Preisklasse, 0,1 W bis 1 W	binär, zunehmend µP-kompatible Busschnittstelle parallel und seriell	schneller Datenwandler in der industriellen Steuer- und Regeltechnik, zur Kommunikation und zur Überwachung schneller Vorgänge; störempfindlich
AD-Parallel-Wandler, ein- und zweistufig	binär, 6 bis 12 Bit, 2 ns bis 200 ns, sehr schnell	mittlere bis hohe Preisklasse, 1 W bis 4 W	binär, parallel	Datenwandler für Oszilloskope, Transientenrecorder, zur Digitalisierung von Videosignalen, Kommunikationstechnik, Überwachungstechnik (Radar)
Delta-Sigma-AD-Wandler	8 bis 16 Bit, 2 µs bis 1 s	günstig bei großen Stückzahlen, Verbrauch gering	binär, seriell und parallel	Datenwandler in der Kommunikationstechnik mit digitalem Filter für besondere Anwendungsfälle





flash converter



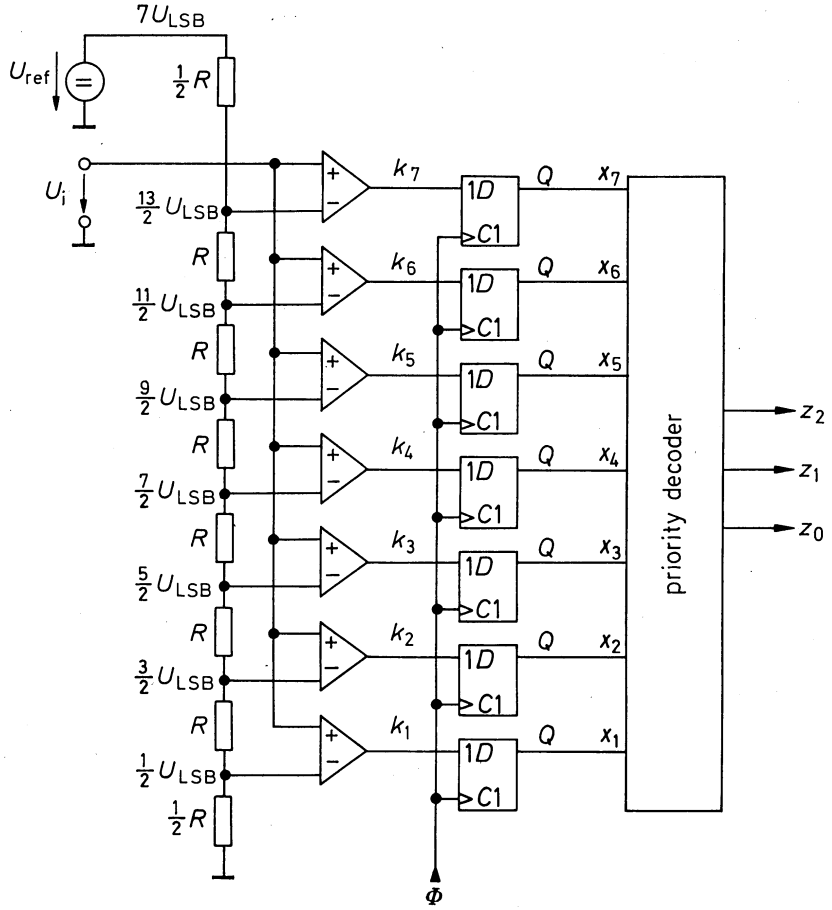
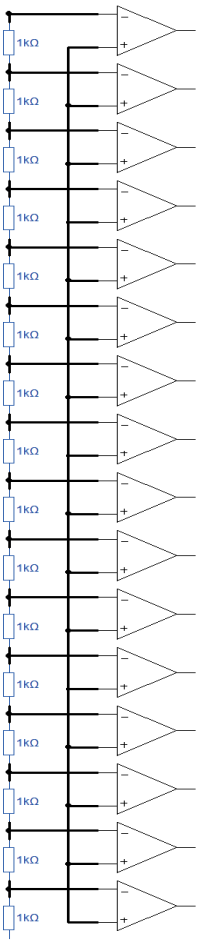


Fig. 23.29 Parallel A/D converter.

$$Z = \frac{U_i}{U_{LSB}} = 7\frac{U_i}{U_{ref}} = Z_{max}\frac{U_i}{U_{ref}}$$

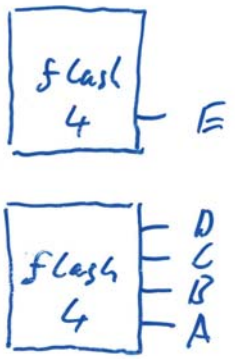
Input voltage	Comparator states							Straight binary number			Decimal equivalent
U_i/U_{LSB}	k_7	k_6	k_5	k_4	k_3	k_2	k_1	z_2	z_1	z_0	Z
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	0	0	1	1
2	0	0	0	0	0	1	1	0	1	0	2
3	0	0	0	0	1	1	1	0	1	1	3
4	0	0	0	1	1	1	1	1	0	0	4
5	0	0	1	1	1	1	1	1	0	1	5
6	0	1	1	1	1	1	1	1	1	0	6
7	1	1	1	1	1	1	1	1	1	1	7

States of variables in the parallel A/D converter as a function of the input voltage



Dezimal	Hexadezimal		
15	F	1 1	1 1
14	E		1 0
13	D		0 1
12	C		0 0
11	B	1 0	1 1
10	A		1 0
9	9		0 1
8	8		0 0
7	7	0 1	1 1
6	6		1 0
5	5		0 1
4	4		0 0
3	3	0 0	1 1
2	2		1 0
1	1		0 1
0	0		0 0

"Seriell" → Binär



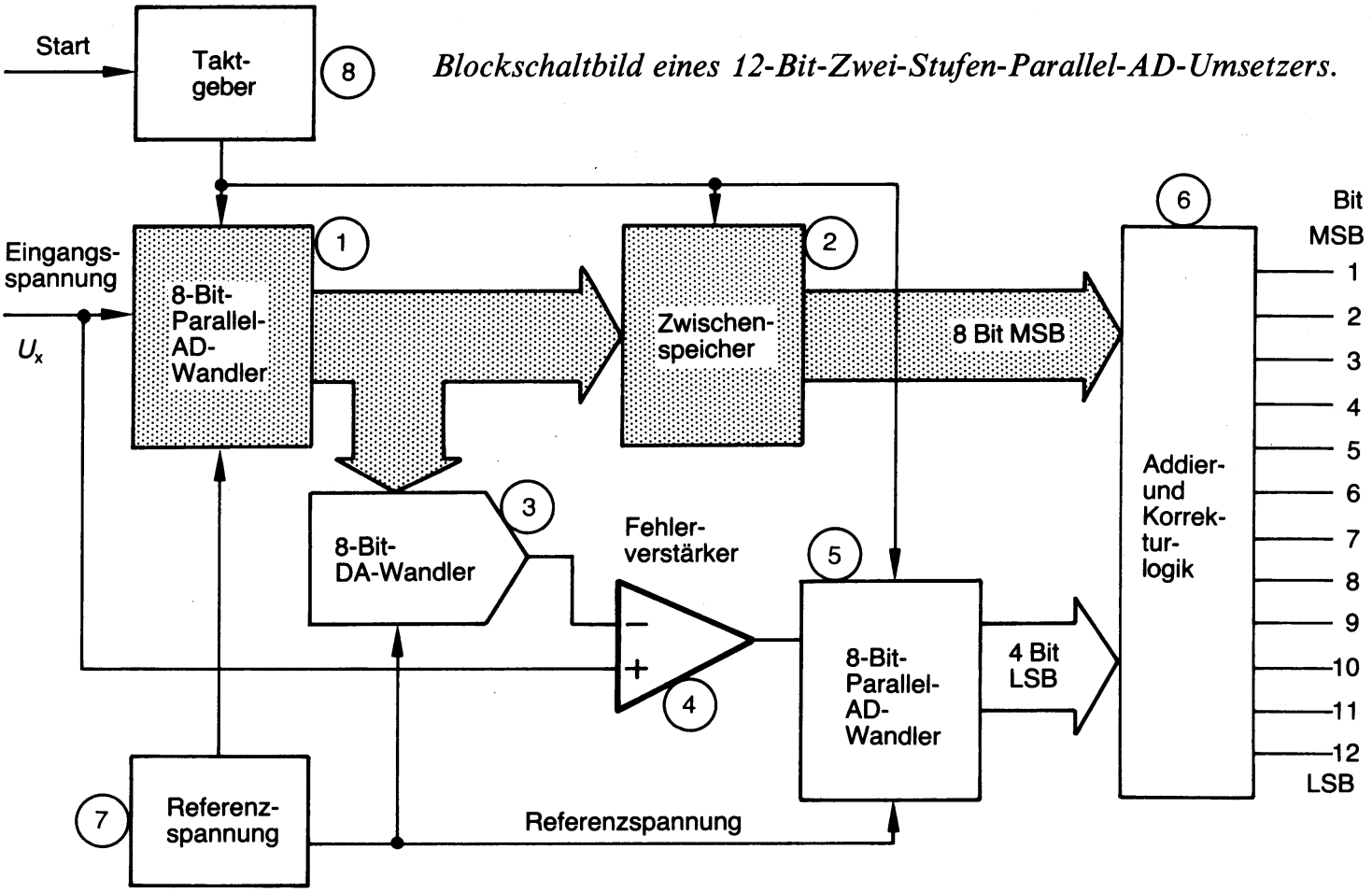
E	1	0 0
D	0	1 1
C	0	1 0
B	0	0 1
A	0	0 0

out 1 out 0

$out1 = CE' = E'C$

$out0 = BC' + DE'$

$= E'D + C'B$



Blockschaltbild eines 12-Bit-Zwei-Stufen-Parallel-AD-Umsetzers.

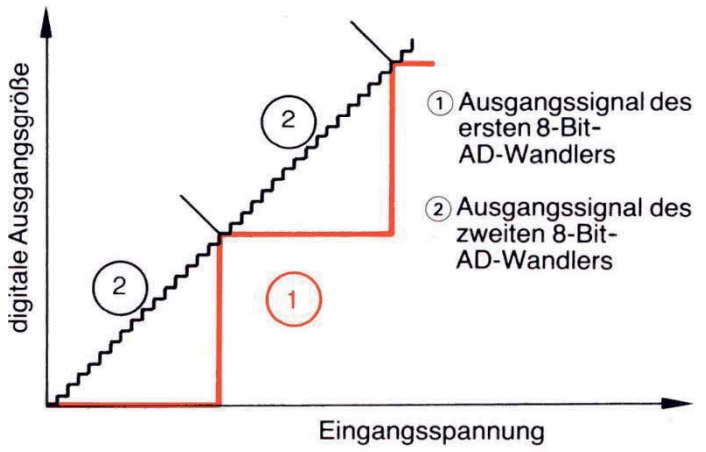


Bild 9-18. Zusammengesetzte Arbeitsbereiche beider Parallelwandler beim Zwei-Stufen-Parallel-AD-Umsetzer.

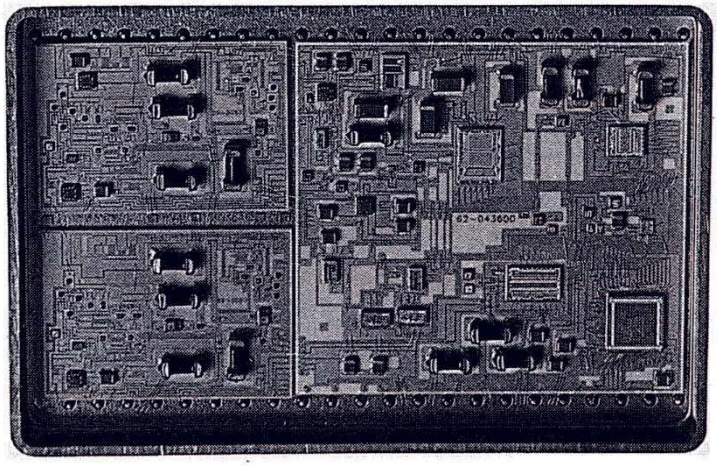


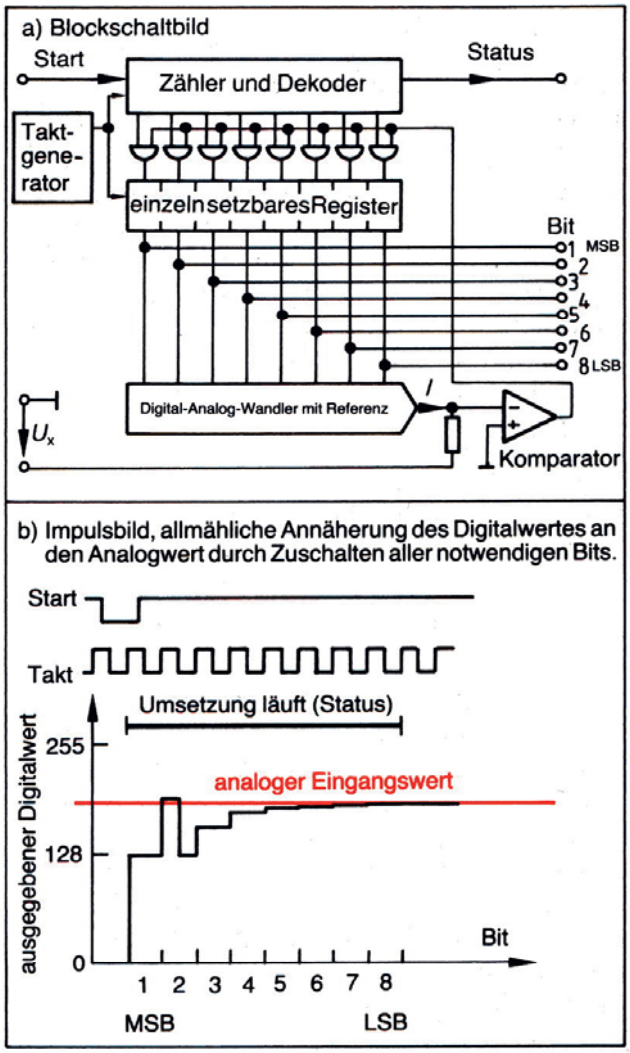
Bild 9-19. Schneller Zweistufen-Parallel-Analog-Digital-Wandler SP9560; 12-Bit, 10 MSPS (leicht vergr.). Werkfoto: Sipex.

Analog-Digital-Wandler

nach dem Prinzip der

sukzessiven

Approximation



Burr-Brown Products
from Texas Instruments

ADS8322

SBAS215 – JULY 2001

16-Bit, 500kHz, MicroPower Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- HIGH-SPEED PARALLEL INTERFACE
- 500kHz SAMPLING RATE
- LOW POWER: 85mW at 500kHz
- INTERNAL 2.5V REFERENCE
- UNIPOLAR INPUT RANGE
- TQFP-32 PACKAGE

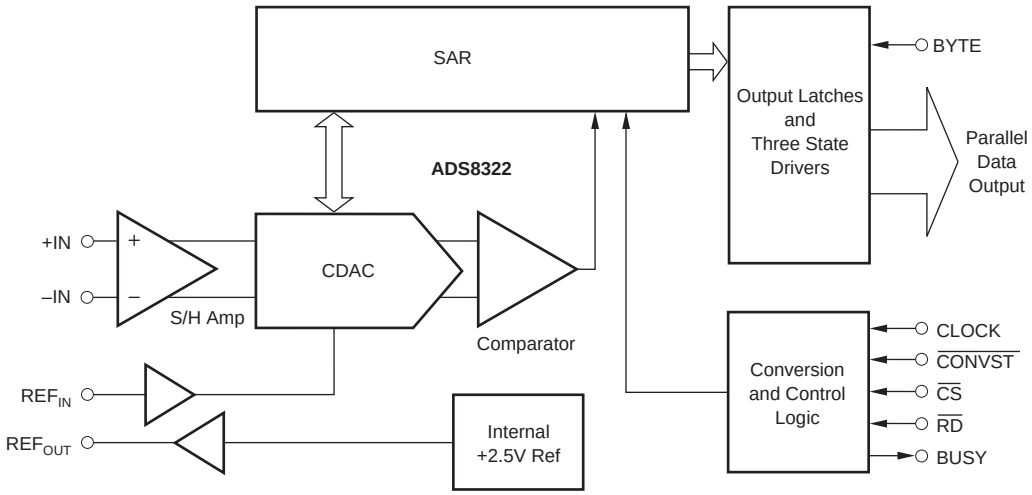
APPLICATIONS

- CT SCANNERS
- HIGH SPEED DATA ACQUISITION
- TEST AND INSTRUMENTATION
- MEDICAL EQUIPMENT

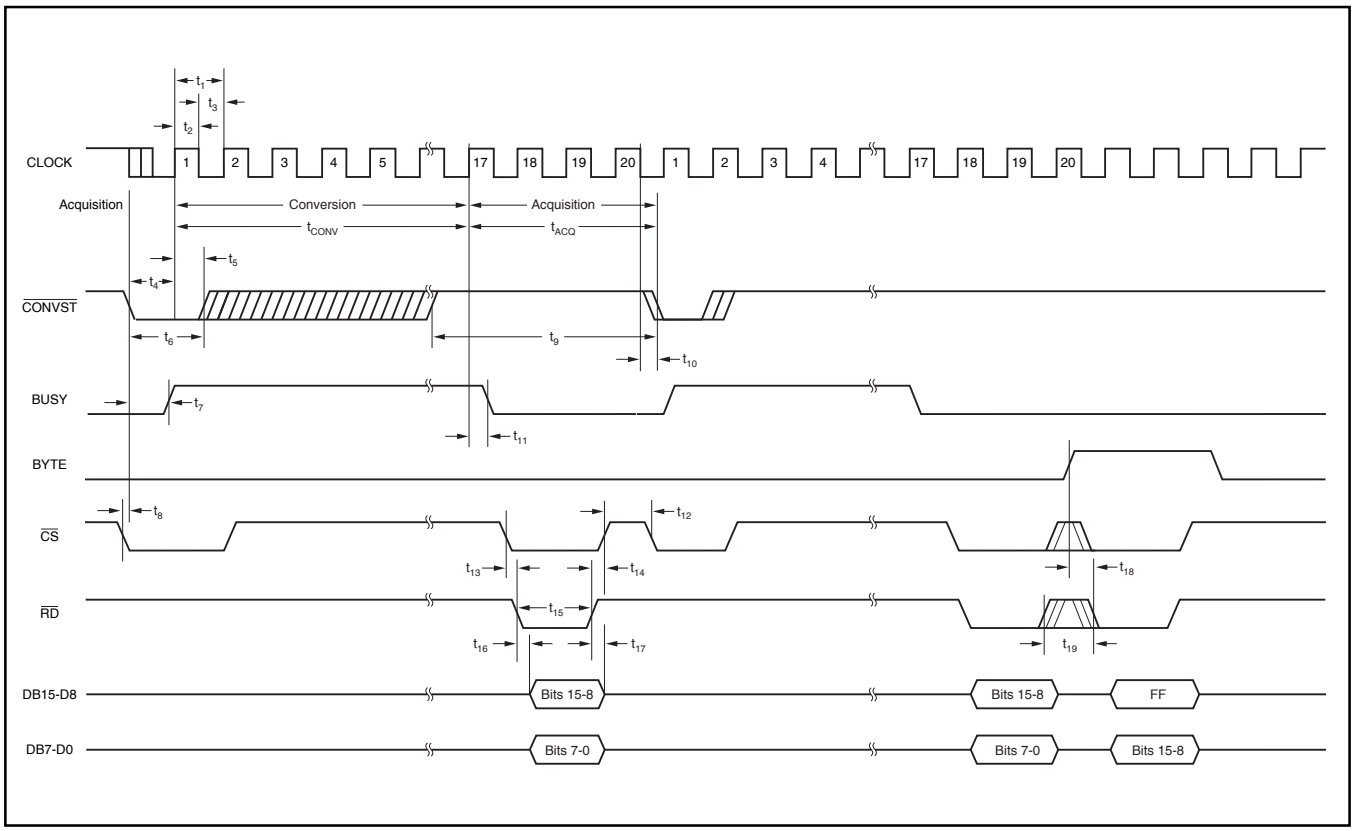
DESCRIPTION

The ADS8322 is a 16-bit, 500kHz Analog-to-Digital (A/D) converter with an internal 2.5V reference. The device includes a 16-bit capacitor-based Successive Approximation Register (SAR) A/D converter with inherent sample-and-hold. The ADS8322 offers a full 16-bit interface, or an 8-bit option where data is read using two read cycles and 8 pins.

The ADS8322 is available in a TQFP-32 package and is guaranteed over the industrial –40°C to +85°C temperature range.



TIMING DIAGRAM



TIMING CHARACTERISTICS[1][2]

All specifications typical at –40°C to +85°C, $+V_D$ = +5V.

PARAMETER	SYMBOL	ADS8322A			ADS8322B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Conversion Time	t_{CONV}			1.6			*	µs
Acquisition Time	t_{ACQ}			0.4			*	µs
CLOCK Period	t_1	100			*			ns
CLOCK High Time	t_2	40			*			ns
CLOCK Low Time	t_3	40			*			ns
$\overline{CONVST}$ Low to Clock High	t_4	10			*			ns
CLOCK High to $\overline{CONVST}$ High	t_5	5			*			ns
$\overline{CONVST}$ Low Time	t_6	20			*			ns
$\overline{CONVST}$ Low to BUSY High	t_7			25			*	ns
$\overline{CS}$ Low to $\overline{CONVST}$ Low	t_8	0			*			ns
$\overline{CONVST}$ High	t_9	20			*			ns
CLOCK Low to $\overline{CONVST}$ Low	t_{10}	0			*			ns
CLOCK High to BUSY Low	t_{11}			25			*	ns
$\overline{CS}$ High	t_{12}	0			*			ns
$\overline{CS}$ Low to $\overline{RD}$ Low	t_{13}	0			*			ns
$\overline{RD}$ High to $\overline{CS}$ High	t_{14}	0			*			ns
$\overline{RD}$ Low Time	t_{15}	50			*			ns
$\overline{RD}$ Low to Data Valid	t_{16}	40			*			ns
Data Hold from $\overline{RD}$ High	t_{17}	5			*			ns
BYTE Change to $\overline{RD}$ Low[3]	t_{18}	0			*			ns
$\overline{RD}$ High Time	t_{19}	20			*			ns

NOTES: (1) All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. (2) See timing diagram, above. (3) BYTE is asynchronous; when BYTE is 0, bits 15 through 0 appear at DB15-DB0. When BUSY is 1, bits 15 through 8 appear on DB7-DB0. $\overline{RD}$ may remain low between changes in BYTE.

THEORY OF OPERATION

The ADS8322 is a high-speed Successive Approximation Register (SAR) A/D converter with an internal 2.5V bandgap reference. The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The basic operating circuit for the ADS8322 is shown in Figure 1.

The ADS8322 requires an external clock to run the conversion process. The clock can be run continuously or it can be gated to conserve power between conversions. This clock can vary between 25kHz (1.25kHz throughput) and 10MHz (500kHz throughput). The duty cycle of the clock is unimportant as long as the minimum HIGH and LOW times are at least 40ns and the clock period is at least 100ns. The minimum clock frequency is governed by the parasitic leakage of the Capacitive Digital-to-Analog (CDAC) capacitors internal to the ADS8322.

The analog input is provided to two input pins, +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

REFERENCE

Under normal operation, the REF_{OUT} pin should be directly connected to the REF_{IN} pin to provide an internal +2.5V reference to the ADS8322. The ADS8322 can operate, however, with an external reference in the range of 1.5V to 2.6V for a corresponding full-scale range of 3.0V to 5.2V.

The internal reference of the ADS8322 is double-buffered. If the internal reference is used to drive an external load, a buffer is provided between the reference and the load applied to the REF_{OUT} pin (the internal reference can typically source and sink 10µA of current). If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the CDAC capacitors during conversion.

ANALOG INPUT

When the converter enters Hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. The voltage on the –IN input is