ADC12J4000 12-Bit 4 GSPS ADC with Integrated DDC

1 Features

- Excellent Noise and Linearity up to and beyond F_{IN} = 2.7 GHz
- Configurable DDC
- Decimation Factors from 4 to 32 (Complex Baseband Out)
- Raw Output Bandwidth of 1000 MHz at 4x Decimation and 4000 MSPS
- Raw Output Bandwidth of 125 MHz at 32x Decimation and 4000 MSPS
- Bypass Mode for Full Bandwidth Data
- Low Pin-Count-Configurable JESD204B Output Interface
- Automatically Optimized Output Lane Count
- Embedded Low Latency Signal Range Indication
- Low Power Consumption
- **Key Specifications**
  - Max Sampling Rate: 4000 MSPS
  - Min Sampling Rate: 1000 MSPS
  - DDC Output Word Size: 15-Bit Complex (30 bits total)
  - Bypass Output Word Size: 12-Bit Offset Binary
  - Noise Floor: −149 dBFS/Hz or −150 dbm/Hz
  - IMD3: −64 dBc (F_{IN} = 2670 MHz ± 2.5 MHz at −10 dBFS)
  - FPBW (-3 dB): 3.3 GHz
  - NPR: 48.5 dB
  - Supply Voltages: 1.9 and 1.2 V
  - Power Consumption
    - Bypass (4000 MSPS): 2.0 W
    - Decimate by 10 (4000 MSPS): 2 W
    - Power Down Mode: 10 mW

2 Applications

- Multi-Standard 3G and 4G Communication Receivers
- RF-Sampling Software Defined Radio
- Wideband Microwave Backhaul
- Military Communications
- SIGINT
- RADAR and LIDAR
- Wideband Communications
- Test and Measurement

3 Description

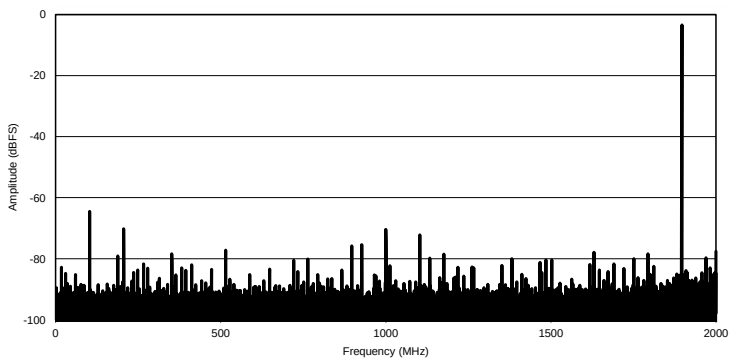
The ADC12J4000 device is a wideband sampling and digital tuning device. The core technology contained in the device is Texas Instruments' giga-sample analog-to-digital converter (ADC) technology that enables a large block of frequency spectrum to be sampled directly at RF. This technology is combined with low-power digital-processing blocks that provide digital filtering and down-conversion. The selected frequency block is made available on a JESD204B serial interface that is compatible with downstream system-processing elements. Data is output as baseband 15-bit complex information for ease of downstream processing. Based on the digital down-converter (DDC) decimation and link output rate settings, this data is output on 1 to 8 lanes of the serial interface.

Device Information

ORDER NUMBER	PACKAGE (PIN)	BODY SIZE
ADC12J4000NKER	QFN (68)	10,00 mm × 10,00 mm

PRODUCT PREVIEW

Bypass — Spectral Response
F_S = 4 GHz, F_{IN} = 1897 MHz



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2014) to Revision A **Page**

- Moved the *Key Specifications* list into the *Features* list 1
- Replaced the *Other Spurs: −81 dBFS* bullet item with *FPBW (–3 dB): 3.3 GHz* bullet item in the *Key Specifications Features* list 1
- Deleted the *under development* statement from the *Description* 1
- Added Table of Contents (*Description (continued)* section now follows the *Revision History)* 1
- Added *Device Information* table 1
- Moved the pin configuration illustration and terminal functions table into a new *Terminal and Configurations* section. Changed Symbol column name to NAME column name 5
- Added the *Device and Documentation Support* section which now contains the trademarks and electrostatic discharge caution 8
- Added the *Mechanical, Packaging, and Orderable Information* section 8

PRODUCT PREVIEW

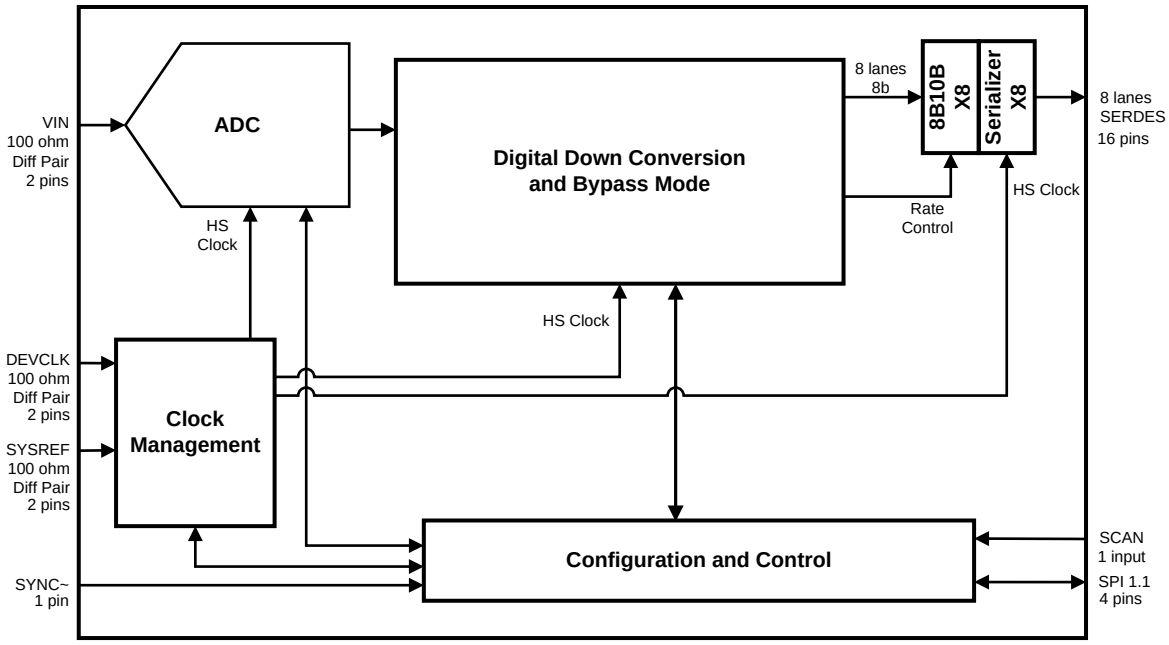
5 Description (Continued)

A DDC bypass mode allows the full rate 12-bit raw ADC data to also be output. This mode of operation requires 8 lanes of serial output.

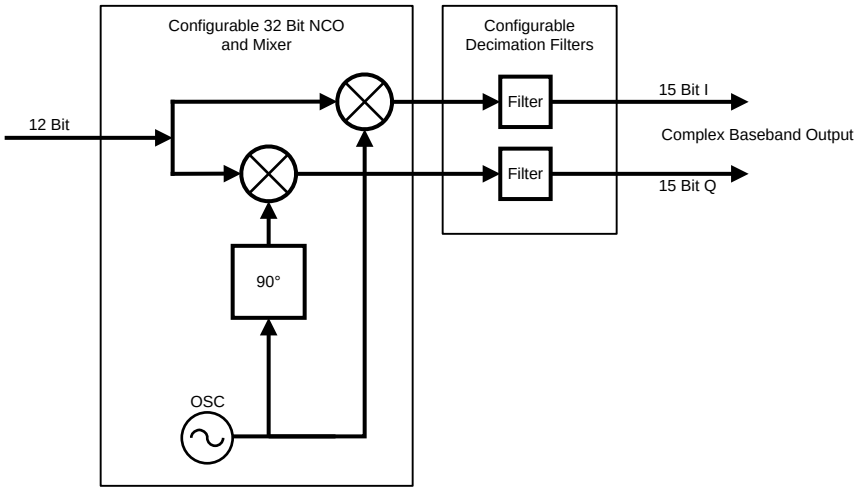
Clear advantages of the ADC12J4000 device over existing solutions currently available on the market are scalability, cost per radio path, power consumption per radio path, and flexibility.

The ADC12J4000 device is available in a 68 terminal QFN package. The device operates over the Industrial ($-40°C \le T_A \le 85°C$) ambient temperature range.

5.1 Block Diagram



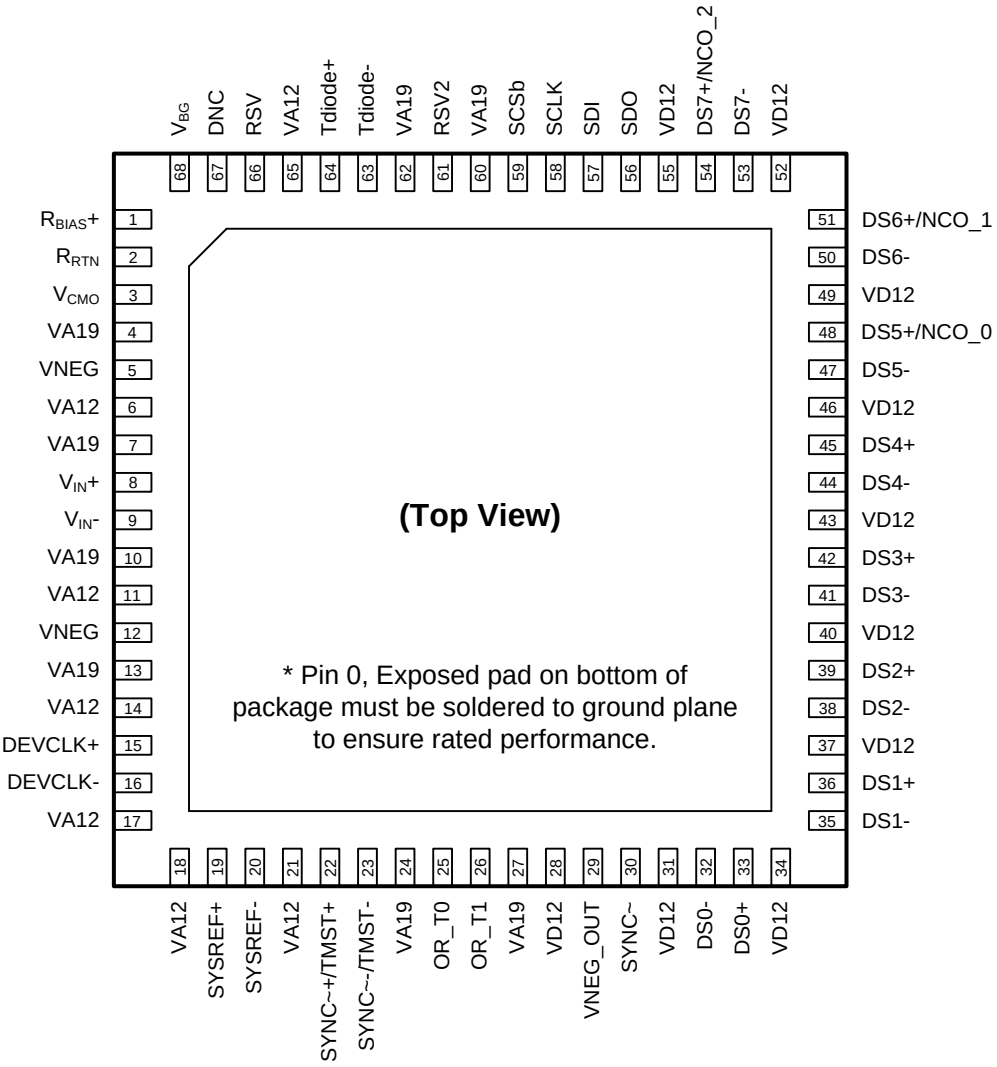
5.2 DDC Details Block Diagram



PRODUCT PREVIEW

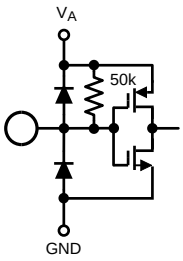
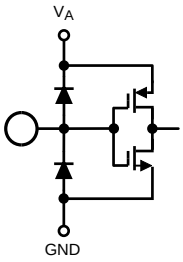
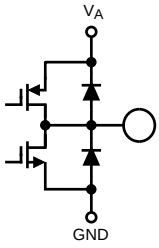
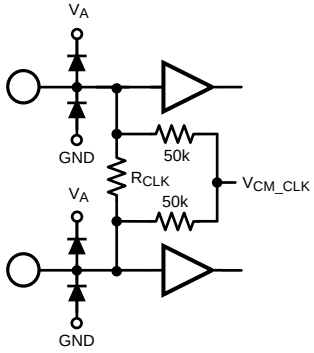
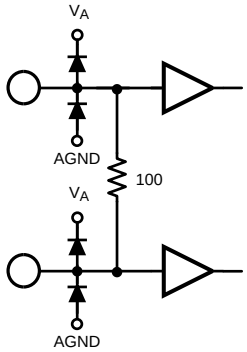
6 Terminal Configuration and Functions

68-Terminal VQFN
NKE Package
(Top View)



*The center pad must be thermally and electrically connected to a ground plane to ensure rated performance.

Terminal Functions

TERMINAL		EQUIVALENT CIRCUIT	DESCRIPTION
NAME	NUMBER		
$\overline{SCS}$	59		**Serial Chip Select (active low)** **(Input): LVCMOS** This terminal functions as the serial-interface chip select. describes the serial interface in more detail.
SCLK	58		**Serial Interface Clock** **(Input): LVCMOS** This terminal functions as the SCLK input which clocks the serial data.
SDI	57		**Serial Data In** **(Input): LVCMOS** This terminal functions as the SDATA input.
SYNC~	30		**SYNC~** **(Input): LVCMOS** This terminal provides the JESD204B-required Synchronizing Request Input. A logic low applied to this input initiates a lane alignment sequence. The choice of LVCMOS or LVDS SYNC~ is selected through the Configuration Register
SDO	56		**Serial Data Out** **Output): LVCMOS** This terminal functions as the SDATA output.
DEVCLK+ DEVCLK−	15 16		**Device Clock Input** **(Input): LVDS** The differential device clock signal must be AC coupled to these terminals. The input signal is sampled on the rising edge of CLK.
SYSREF+ SYSREF−	19 20		**SYSREF** **(Input): LVDS** The differential periodic waveform on these terminals synchronizes the device per JESD204B.
SYNC~+/TMST+ SYNC~-/TMST-	22 23		**SYNC~/TMST** **(Input): LVDS** This differential input provides the JESD204B-required Synchronizing Request Input. A differential logic low applied to these inputs initiates a lane alignment sequence. The choice of LVCMOS or LVDS SYNC~ is selected through the Configuration Register When the LVCMOS SYNC~ is selected and configured through the Configuration Register 0x202h, bit 6, these inputs are the differential TIMESTAMP input. For additional information see the section.

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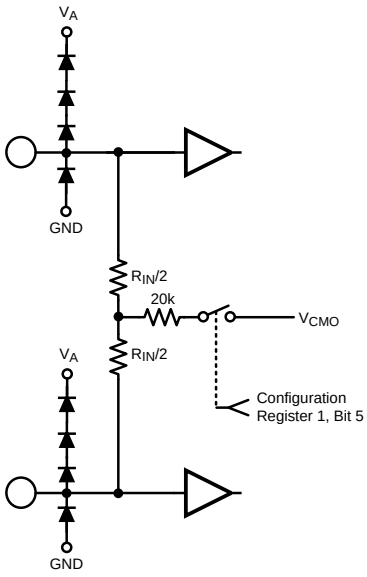
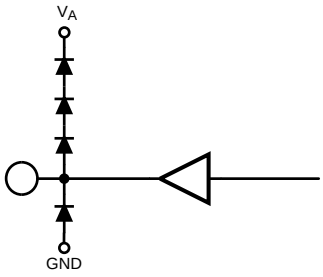
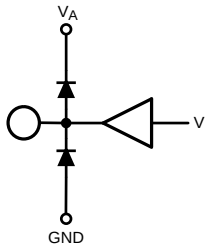
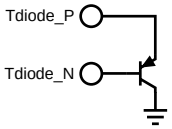
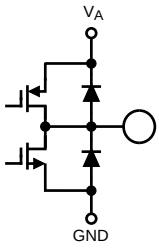
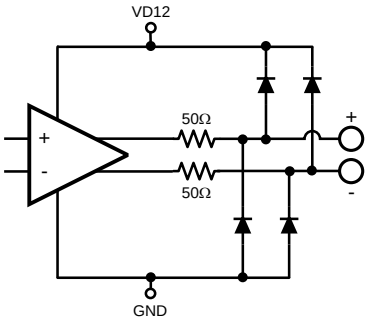
Terminal Functions (continued)

TERMINAL		EQUIVALENT CIRCUIT	DESCRIPTION
NAME	NUMBER		
V_{IN}+ V_{IN}−	8 9		**Signal Input** **(Input): Analog** The differential full-scale input range is determined by the Full-Scale Voltage Adjust register.
V_{CMO}	3		**Common Mode Voltage** **(Output): Analog** The voltage output at this terminal must be the common-mode input voltage at V_{IN}+ and V_{IN}− when DC coupling is used. This terminal is capable of sourcing or sinking 100 µA and can drive a load up to 80 pF.
V_{BG}	68		**Bandgap Output Voltage** **(Output): Analog** This terminal is capable of sourcing or sinking 100 µA and can drive a load up to 80 pF.
R_{BIAS}+	1		**External Bias Resistor Connection** **(Output): Analog** The nominal value of R_{BIAS}+ is 3.3 kΩ (±0.1%) to the R_{RTN} terminal.
R_{RTN}	2		**Bias Resistor Return** **(Input): Analog** This terminal is the return input for external R_{BIAS}. This terminal must be isolated from all other signals and grounds. DO NOT CONNECT TO GROUND.
Tdiode+ Tdiode−	64 63		**Temperature Diode** **(Passive): Analog** These terminals are the positive (Anode) and negative (Cathode) diode connections for die temperature measurements.

Terminal Functions (continued)

TERMINAL		EQUIVALENT CIRCUIT	DESCRIPTION
NAME	NUMBER		
OR_T0 OR_T1	25 26		**Over-Range** **(Output): LVCMOS** OverRange Detection Status for T0 and T1 thresholds.
DS0+ / DS0− DS1+ / DS1− DS2+ / DS2− DS3+ / DS3− DS4+ / DS4− *DS5+ / DS5− *DS6+ / DS6− *DS7+ / DS7−	33 / 32 36 / 35 39 / 38 42 / 41 45 / 44 48 / 47 51 / 50 54 / 53		**Data** **(Output): CML** These terminals are the high-speed serialized-data outputs with user-configurable pre-emphasis. These outputs must always be terminated with a 100-Ω differential resistor at the receiver. **DS5+, DS6+ and DS7+**: When decimation is enabled, these terminals become LVCMOS inputs and allow the host device to select the specific NCO Frequency/Phase accumulator that is active.
VNEG_OUT	29		**VNEG_OUT** **(Output): Power** This power output terminal must be decoupled with a 4.7-µF capacitor to ground and connected to the VNEG input terminals.
VNEG	5 12		**VNEG** **(Input): Power** This terminal must be decoupled to ground with a 0.1-µF capacitor near each terminal. These power input terminals must be connected to the VNEG_OUT terminal. The connections must be isolated from any noisy digital signals and must also be isolated from the analog input and clock input terminals.
VA19	4, 7, 10, 13, 24, 27, 60, 62		**Analog 1.9-V power supply terminals** **(Power)** – Bypass these terminals to ground using one 10-µF and two 1-µF capacitors for bulk decoupling plus one 0.1-µF capacitor per terminal for individual decoupling.
VA12	6, 11, 14, 17, 18, 21, 65		**Analog 1.2-V power supply terminals** **(Power)** – Bypass these terminals to ground using one 10-µF and two 1-µF capacitors for bulk decoupling plus one 0.1-µF capacitor per terminal for individual decoupling.
VD12	28, 31, 34, 37, 40, 43, 46, 49, 52, 55		**Digital 1.2-V power supply terminals** **(Power)** - Bypass these terminals to ground.
GND	0		**Ground** - Terminal 0 is the exposed pad on the bottom of the package and is the ground return for all supplies. This terminal/pad must be connected with multiple vias to the printed circuit board (PCB) ground planes to ensure proper electrical and thermal performance.
RSV2	61		**Connect to Ground** - Connect this reserved terminal to ground for proper operation.
RSV	66		**Reserved** - Do not connect RSV to any circuitry, power, or ground signals.
DNC	67		**Do Not Connect** - Do not connect DNC to any circuitry, power, or ground signals.

PRODUCT PREVIEW

7 Device and Documentation Support

7.1 Trademarks

All trademarks are the property of their respective owners.

7.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

7.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

8 Mechanical, Packaging, and Orderable Information

The following packaging information and addendum reflect the most current data available for the designated devices. This data is subject to change without notice and revision of this document.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC12J4000NKER	PREVIEW	VQFN	NKE	68	2000	TBD	Call TI	Call TI	-40 to 85		
ADC12J4000NKET	PREVIEW	VQFN	NKE	68	250	TBD	Call TI	Call TI	-40 to 85		
PADC12J4000NKE	PREVIEW	VQFN	NKE	68	1	TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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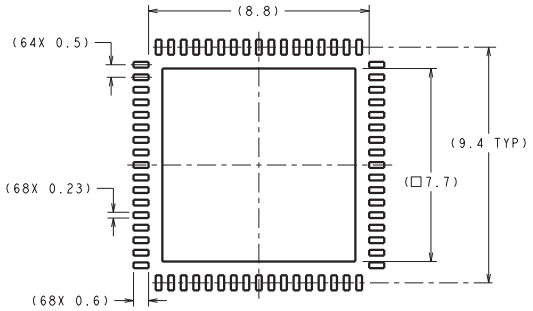
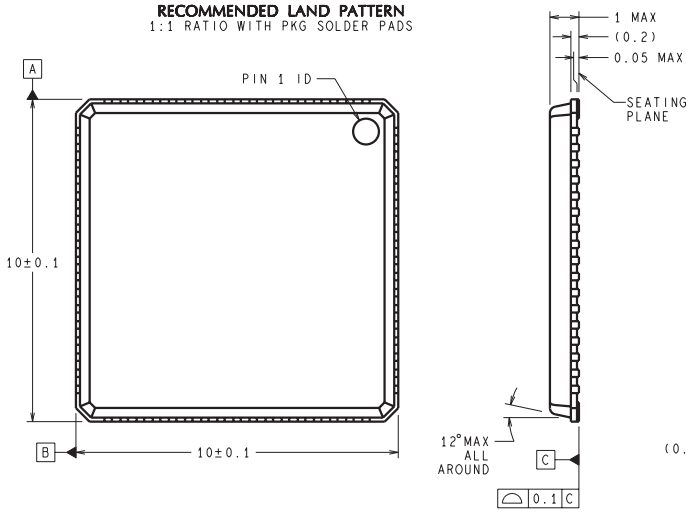
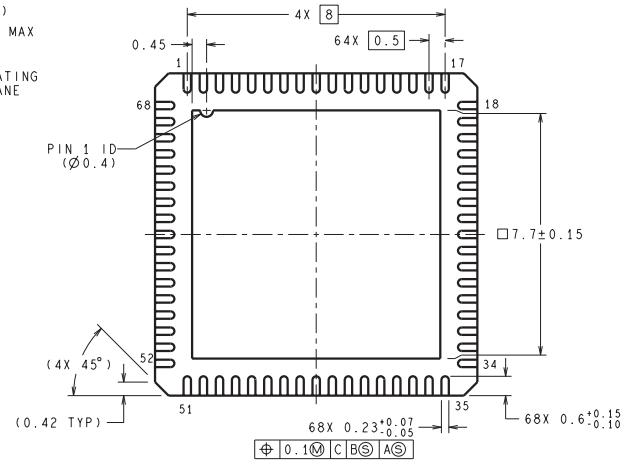


RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





LQA68A (Rev B)

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